Multiphase Digital Pulsewidth Modulator

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Abstract—This letter describes a digital pulsewidth modulator that enables the generation of a large, adjustable number of pulsewidth modulated (PWM) outputs of programmable duty cycle and dead time, yet requiring just a small, fixed architecture. The design achieves a resolution of 255 ps using a composite PWM strategy that also minimizes clock frequency and area. It provides a practical solution to the problem of efficiently generating multiple high-resolution gate-drive signals and is particularly suited to the next generation of synchronously switched multiphase voltage regulator modules.

Index Terms—DC–DC power conversion, digital control, field-programmable gate arrays (FPGA), switched-mode power supplies.

I. INTRODUCTION

D IGITAL methods are being used with increasing frequency in the field of power electronics [1], enabling designers to meet evolving performance specifications, achieve improved efficiency, and implement additional functionality with greater ease. In particular, it is expected that digital control will be the regulation method of choice for voltage regulator modules (VRMs) in the near future [2]. This letter deals with a key issue in digital VRM control—pulsewidth modulation (PWM)—approached from the perspectives of area-efficiency and enhanced resolution. A novel multiphase digital pulsewidth modulator (DPWM) is proposed. It uses a small, fixed architecture to generate high-resolution versatile gate-drive signals and incorporates on-line calibration circuitry. Experimental verification using a field-programmable gate arrays (FPGA) is also described.

II. HIGH RESOLUTION TIMING GENERATION

A. Existing Architectures

Counter-comparator [3], [4] and delay-line [5], [6] methods have been used to generate PWM signals. Unfortunately, these methods can be unsuited to very-high-resolution applications since either an excessive clock frequency or implementation area is needed. Techniques such as dithering [7] and \( \Sigma – \Delta \) PWM [8] can improve the time-averaged resolution but may add an extra ac ripple to the converter output. Instead, the hybrid counter-with-delay-line approach of [9], [10] seems to reach a good compromise between area, clock frequency and resolution. However, even this approach reaches a practical limit in terms of area and clock frequency as the underlying resolution is increased.

B. Heterogeneous DPWM

An \( r \)-to-1 multiplexer/delay-line (MDL) pair may be decomposed into a logically equivalent chain of \( m \times 2^p \)-to-1 MDL pairs, where \( \sum_{i=1}^{m} p_i = r \). The index \( i \) represents the position of a pair in the chain from output \( (i = 1) \) to input \( (i = m) \). The total distributed multiplexer (MUX) area may be quantified in terms of primitive 2-to-1 MUX components. Here

\[
A_{MUX} = \sum_{i=1}^{m} 2^{p_i} - 1
\]  

(1)

where \( 2^{p_i} - 1 \) is the number of 2-to-1 primitives required to implement each \( 2^{p_i} \)-to-1 MUX. The number of delay elements at any level of the MDL chain may be found using the recursion

\[
d_i = d_{i-1} \cdot 2^{p_i}, \quad i = 1, 2, \ldots, m
\]  

(2)

where \( d_0 = 1 \). The total number of distributed delay elements is therefore

\[
A_{DE} = \sum_{i=1}^{m} d_i
\]  

(3)

A tree displaying all the possible implementations of an 8-to-1 MDL decomposition is shown in Fig. 1. It may be shown that \( A_{DL} \) is minimized and \( A_{MUX} \) maximized when \( m = 1 \), i.e., no decomposition of the original MDL pair, while \( A_{DL} \) is maximized and \( A_{MUX} \) minimized when \( p_1 = p_2 = \cdots = p_m = 1 \), i.e., \( m = r \) implying full decomposition.

This tradeoff is the key to minimizing the area of the pulsewidth modulator: a semi-decomposed structure is required whose elements are chosen to satisfy area, linearity and monotonicity criteria. When the area consumed by a single delay element is comparable to that required to implement a MUX primitive, an area-minimizing decomposition may be:

Fig. 1. Possible implementations of an 8-to-1 MDL decomposition, showing \( A_{DE} \) and \( A_{MUX} \) totals for each branch.
Duty Cycle  \[ j \cdot \delta_j \]

Counter/comparator

Comparator

\[ '111...1' \]

A = B

Fig. 2. Heterogeneous DPWM architecture.

4-bit ring-oscillator delay-line and MUX

1-bit auxiliary delay-line

PWM Output

10-bit (5)

Area

15

10

100

1

k

7

Fig. 3. Area tradeoff between ring oscillator/MUX (k-bit) and auxiliary delay line (I-bit). The minimum area occurs when \( k = i \).

The timing-generation circuit consists of four heterogeneous DPWMs. Each sub-DPWM is required to have identical timing characteristics, because it is desirable that the outputs be accurately matched. To achieve this, just one delay line is used to establish all timing events—further optimizing the area. In each switching cycle, the memory is updated with an array of event-data vectors, representing the required switching instants of each of the converter’s \( N \) phases. This data is grouped by event type and fed to one of the four sub buses of the bus array, \( d \), such that a sub bus carries data corresponding to just one

\[ \phi = \frac{1}{f_{\text{sw}} \cdot N} \]  

(5)

where \( f_{\text{sw}} \) is the switching frequency. Though there are many individual switching events per period, there are just four distinct event types: \( Q_{\text{x}_{\text{on}}} \), \( Q_{\text{x}_{\text{of}}} \), \( S_{\text{x}_{\text{on}}} \), and \( S_{\text{x}_{\text{of}}} \), as shown in Fig. 4. Each event type occurs in an ordered sequence—a fact that can be exploited to facilitate asynchronous time sharing of timing-generation components, rather than using a separate, area-intensive dedicated timing generator for each edge/phase, as has been done up to now [5], [9], [13]. The architecture shown in Fig. 5 is used to accomplish this [11].

III. MULTIPHASE PULSWEIDTH MODULATOR

In an \( N \)-phase interleaved quasi-square-wave buck converter [12], with phase separation of \( \phi \) seconds and duty-cycles in each phase assumed to be equal, it follows, in general, that

\[ Q_{x+1}(t + \phi) = Q_{x}(t) \]

\[ S_{x+1}(t + \phi) = S_{x}(t), \quad x = 1, 2, \ldots, N \]  

(4)

where \( Q_{x}(t) \) and \( S_{x}(t) \) are the respective instantaneous values of the top- and bottom-switch gate-drive signals in phase \( x \), and
event type. Each sub bus is updated \( N \) times per cycle when its memory bank is incremented (via the event bus) due to the previous event of the same type having been resolved, i.e., a pulse is generated at the output of the corresponding "AND" gate. Each signal of the event bus is a train of pulses that must be directed to the correct \( S \) or \( R \) ports of the \( 2N \) output latches to generate the PWM waveforms. This is done using four 1-to-\( N \) counters, which keep track of each of the event bus signals. When a counter output is decoded into a 1-of-\( N \) format, the resulting signals may be used to enable the \( S \) or \( R \) port of a particular output latch before its next expected event.

The only practical limit to the number of phases is the finite time, \( \tau \), it takes to increment the memory from one value to the next. For correct operation \( \tau < \phi \). In this implementation the 1-to-\( N \) counters have a maximum value of \( N \), which may be set by the user, enabling the number of output phases to be adjusted either dynamically, for phase shedding at light loads, or on an application-specific basis. The average frequency of these counters is equal to the product of the number of phases and the converter switching frequency.

### IV. Calibration

If the rising edge of signal \( Q_1(t) \) is viewed as the time origin in each period, each subsequent event in the switching cycle occurs some programmable interval thereafter—including the next rising edge of the signal itself. By detecting this edge and resetting the main counter and the ring oscillator at this instant, a new cycle is initiated. Thus, the circuit behaves like a digitally controlled oscillator (DCO). Since the switching period is now programmable, variable frequency operation is accomplished. The range of possible switching frequencies, \( f_{SW} \), is

\[
\frac{1}{\delta \cdot 2^s} \leq f_{SW} \leq \frac{1}{N + \tau}
\]  

(6)

where \( \delta \) is the latency of a single auxiliary delay-line component and \( s \) is the aggregate number of bits of resolution of each sub-DPWM circuit.

Frequency calibration is achieved using an all-digital phase locked loop (DPLL), which may be constructed using a DCO, an up-down counter (acting as a loop filter, the output of which determines the switching period) and a digital phase detector (DPD) [14], as shown in Fig. 6. The DPD used here compares the phases of the rising edge of \( Q_1(t) \) and a reference clock. When it is detected that there are two or more \( Q_1(t) \) rising edges per period of the reference clock then the up-down counter is incremented, thus reducing the frequency of the DCO. The DCO frequency is increased when there is one \( Q_1(t) \) rising edge (or none) per period of the reference clock [15]. When both signals have locked, the switching period varies within a range of adjacent values, resulting in jitter, and thus inaccuracy, in the calibration cycle. This is due to the simple phase detector circuit having a single output (\( \text{up}/\text{down} \)) so that the counter output enters a limit cycle oscillation or near lock. This is exacerbated by the asynchronous reset used in the DPD, the effect of which is most acute near to lock when the reference clock and \( Q_1(t) \) edges occur almost simultaneously: timing violations then cause the \( \text{up}/\text{down} \) signal to be resolved incorrectly. This results in limited, though discernible, excursions about the ideal switching period value. However, the magnitude of this jitter has been measured to be within the tolerances of typical VRM output filter components, so its effect may be disregarded in this application.

### V. Experimental Verification

The multiphase heterogeneous-DPWM architecture described in this letter has been implemented on a Xilinx Virtex XC2V3000-4FG676 FPGA. The 32-element ring-oscillator delay lines were constructed using the dedicated flip-flops available on this device. These have a latency of approximately 1 ns, measured at a die temperature of 30 °C. This time interval is further divided into finer-grain increments, with an average value of 255 ps at the same temperature, using the auxiliary delay stages, thus providing 11 b of resolution at a switching frequency of approximately 1.9 MHz. These fine time increments are illustrated in Fig. 7, where a sequence of five top-switch falling edges are shown as the duty-cycle is changed between a number of consecutive values. The variation of output frequency with temperature is of interest, since the ambient temperature in which the circuit should operate can vary substantially. This has been investigated using an on-die temperature sensor with ambient heating, and the
Fig. 7. Waveforms numbered 1–5 show the falling edge of a single top-switch output as the duty cycle is varied between five consecutive values, thus demonstrating the high resolution of the heterogeneous-DPWM architecture.

Fig. 8. Normalized output frequency response versus die temperature.

frequency-to-temperature response of the circuit, normalized at 30 °C, is shown in Fig. 8. At approximately 0.11% per °C, the measurements correspond well to similar experiments in the literature [16]. However, calibration of the delay line during normal operation may be used to overcome the temperature dependency of the output frequency.

The DPWM was configured to eight phases to demonstrate a typical output, shown in Fig. 9—a screen shot of a logic analyzer display, showing 16 top- and bottom-switch gate-drive waveforms. The number of phases is not confined to this value, however, and may be adjusted as required. The eight-phase design (excluding the memory) is fully implemented in just 203 LUTs, and careful multiplexer placement using interleaving techniques ensures monotonicity and excellent linearity. The required implementation area is approximately 3/(2N) of that of an architecture not optimized in this way, where, again, N is the number of converter phases. Some performance figures for this circuit are summarized in Table I.

Fig. 9. Pulswidth modulated output of the implemented eight-phase heterogeneous DPWM operating at a switching frequency of 1.9084 Mhz per phase.

TABLE I
SUMMARY OF CIRCUIT PERFORMANCE

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ring-oscillator delay line</td>
<td>No. of delay cells 32</td>
</tr>
<tr>
<td>Typical cell latency</td>
<td>~ 1.02 ns</td>
</tr>
<tr>
<td>Total line delay</td>
<td>~ 32.75 ns</td>
</tr>
<tr>
<td>Auxiliary delay line</td>
<td>No. of delay cells 3</td>
</tr>
<tr>
<td>Average cell latency</td>
<td>~ 255 ps</td>
</tr>
<tr>
<td>Total line delay</td>
<td>~ 765 ps</td>
</tr>
<tr>
<td>Memory increment delay</td>
<td>τ</td>
</tr>
<tr>
<td>Resolution @ 15 MHz</td>
<td>0.255%</td>
</tr>
<tr>
<td>Resolution @ 1.9084 MHz</td>
<td>0.0488%</td>
</tr>
<tr>
<td>ADPLL calibration time</td>
<td>~ 1.5 ms</td>
</tr>
<tr>
<td>Peak ADPLL jitter</td>
<td>1.7%</td>
</tr>
</tbody>
</table>

VI. CONCLUSION

A multi-output DPWM has been introduced for use with multiphase interleaved dc–dc buck converters, generating versatile waveforms with variable switching frequency, programmable dead times, adjustable phasing and online calibration capability. This is achieved using a novel architecture that also exploits the phased nature of the switching signals required by this topology to minimize the overall area consumed. The heterogeneous-DPWM structure, on which the design is based, achieves a resolution of 255 ps, but without a large clock-frequency or silicon-area requirement.

REFERENCES


