AC/DC/AC Converters:
Two-Level and Multilevel VSI

Josep Pou
Antoni Arias

Outline

1. Two-Level Inverter
2. Multilevel Inverters
   - Cascade H-Bridge Inverter
   - Flying-Capacitor Inverter
   - Diode-Clamped Inverter
3. Back-to-Back Connection

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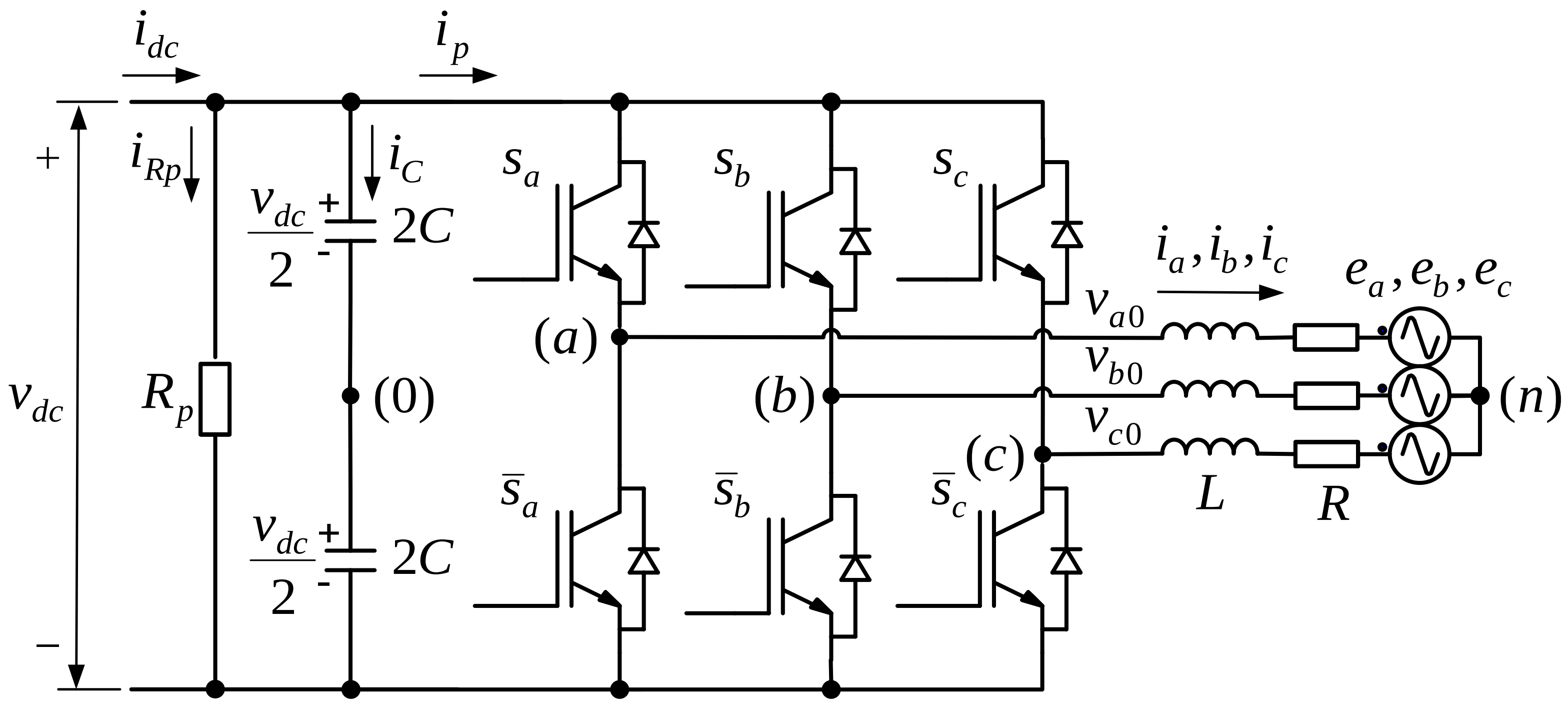
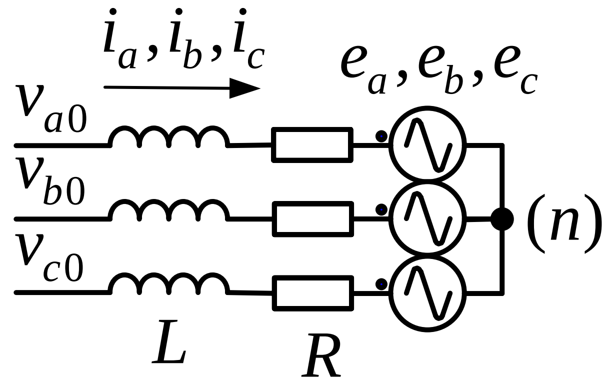
1. Two-Level Three-Phase Inverter

Grid-connected inverter



Modeling the AC Side

$$\begin{cases} v_{a0} = L\dfrac{di_a}{dt} + R\,i_a + e_a + v_{n0} \\ v_{b0} = L\dfrac{di_b}{dt} + R\,i_b + e_b + v_{n0} \\ v_{c0} = L\dfrac{di_c}{dt} + R\,i_c + e_c + v_{n0} \end{cases}$$



$+$

$$v_{a0} + v_{b0} + v_{c0} = L\frac{d(i_a + i_b + i_c)}{dt} + R(i_a + i_b + i_c) + e_a + e_b + e_c + 3v_{n0}$$

$$i_a + i_b + i_c = 0$$

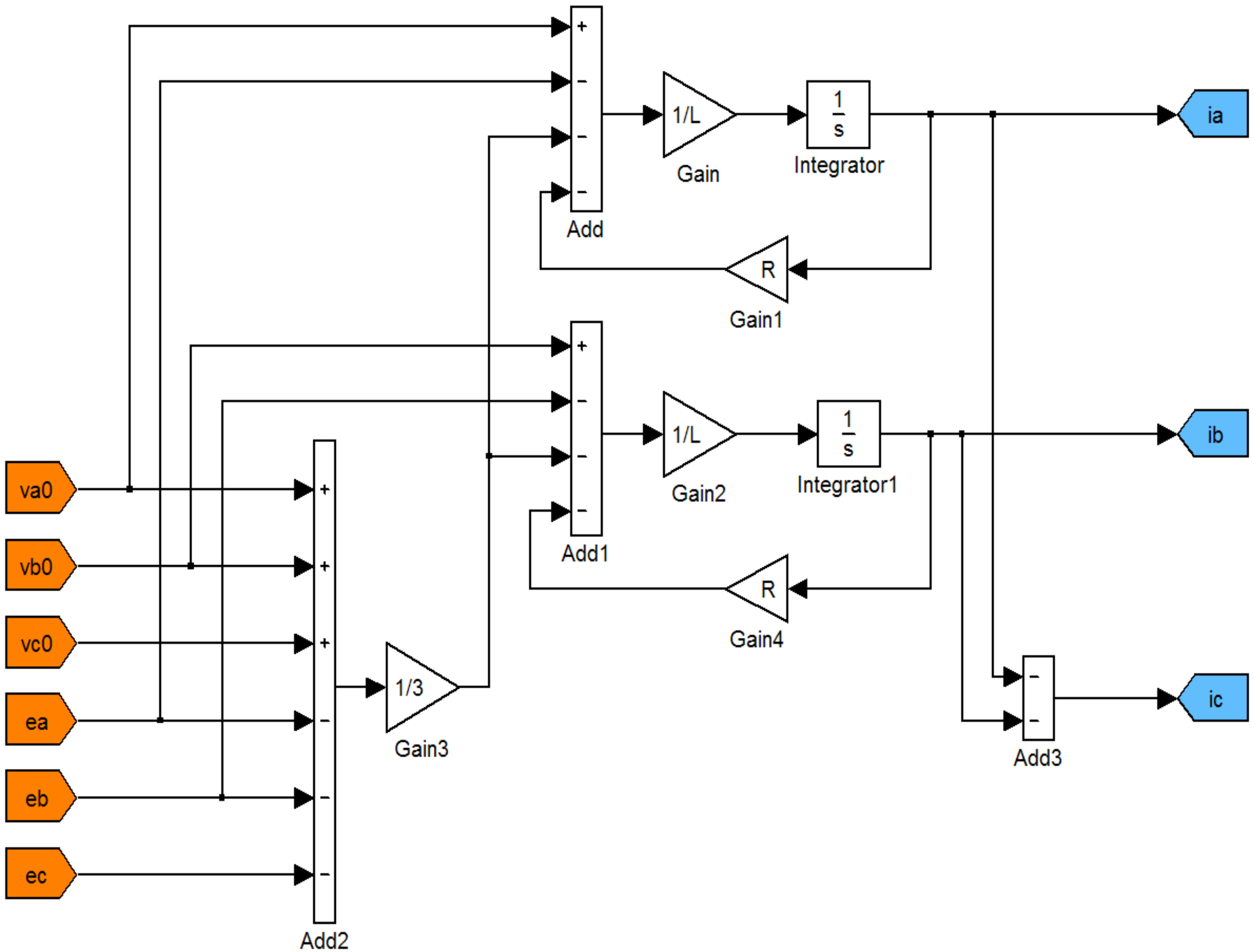
$$v_{n0} = \frac{v_{a0} + v_{b0} + v_{c0} - (e_a + e_b + e_c)}{3}$$

Modeling the AC Side

$$\begin{cases} \dfrac{di_a}{dt} = \dfrac{1}{L}\left(v_{a0} - R\,i_a - e_a - v_{n0}\right) \\ \dfrac{di_b}{dt} = \dfrac{1}{L}\left(v_{b0} - R\,i_b - e_b - v_{n0}\right) \\ \dfrac{di_c}{dt} = \dfrac{1}{L}\left(v_{c0} - R\,i_c - e_c - v_{n0}\right) \end{cases}$$

$$\begin{cases} i_a = \int di_a = \int \dfrac{1}{L}\left(v_{a0} - R\,i_a - e_a - v_{n0}\right)dt \\ i_b = \int di_b = \int \dfrac{1}{L}\left(v_{b0} - R\,i_b - e_b - v_{n0}\right)dt \\ i_c = -i_a - i_b \end{cases}$$

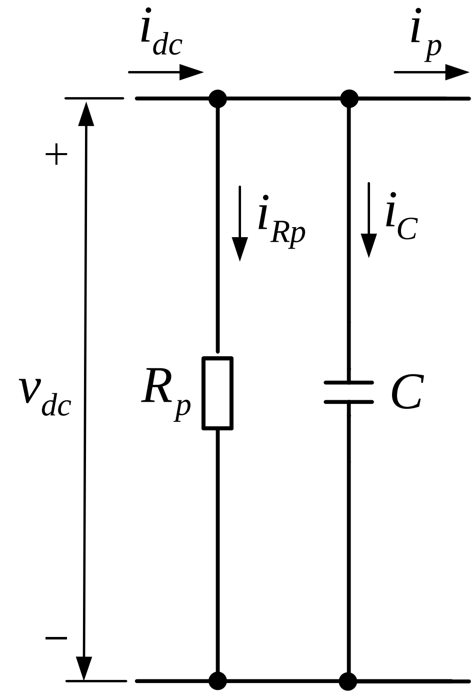
Matlab-Simulink Model



Modeling the DC Side

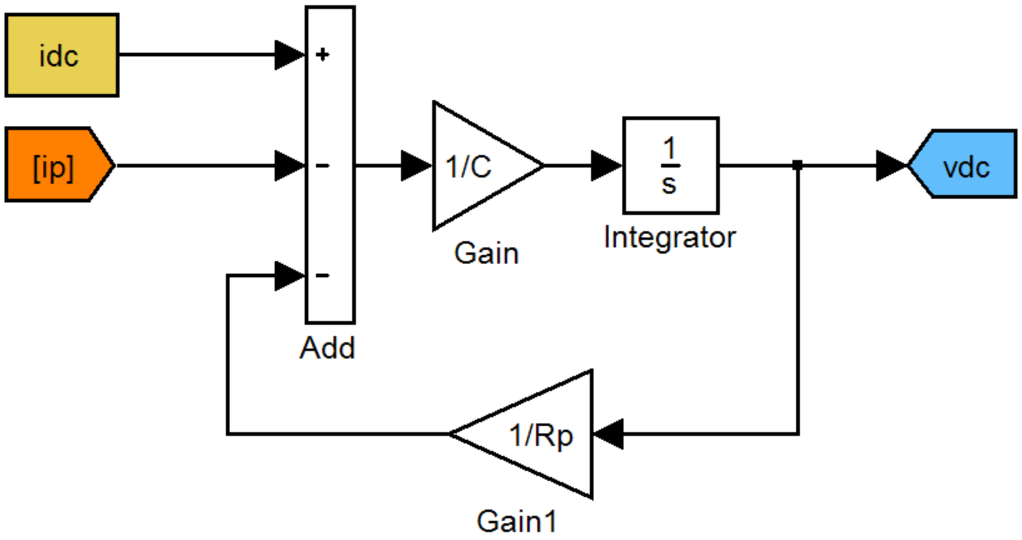
$$\begin{cases} i_C = i_{dc} - i_{Rp} - i_p = C\dfrac{dv_{dc}}{dt} \\ i_{Rp} = \dfrac{v_{dc}}{R_p} \end{cases}$$

$$\frac{dv_{dc}}{dt} = \frac{1}{C}\left(i_{dc} - \frac{v_{dc}}{R_p} - i_p\right)$$



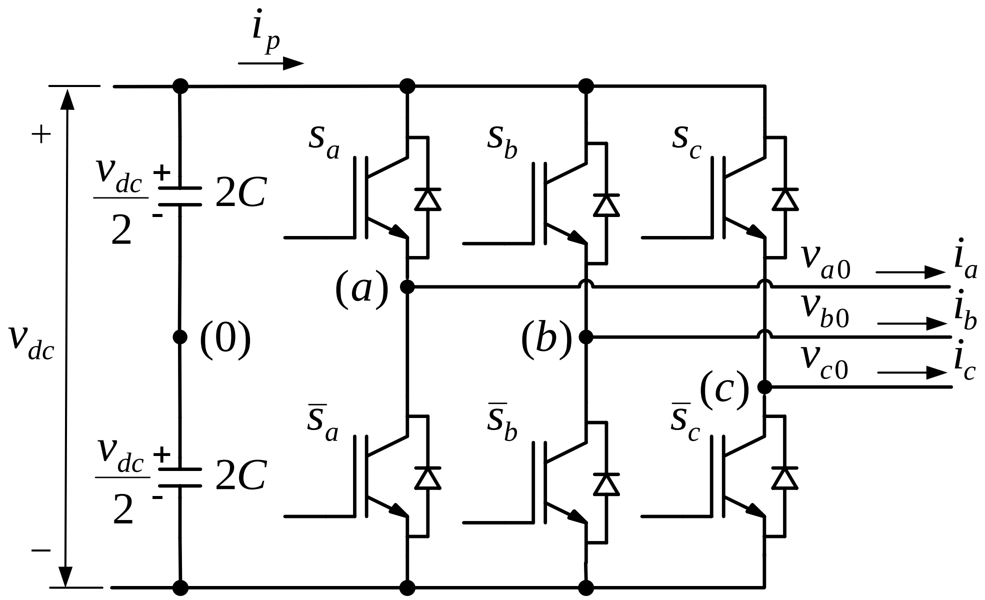
Matlab-Simulink Model

$$v_{dc} = \int dv_{dc} = \int \frac{1}{C}\left(i_{dc} - \frac{v_{dc}}{R_p} - i_p\right)dt$$

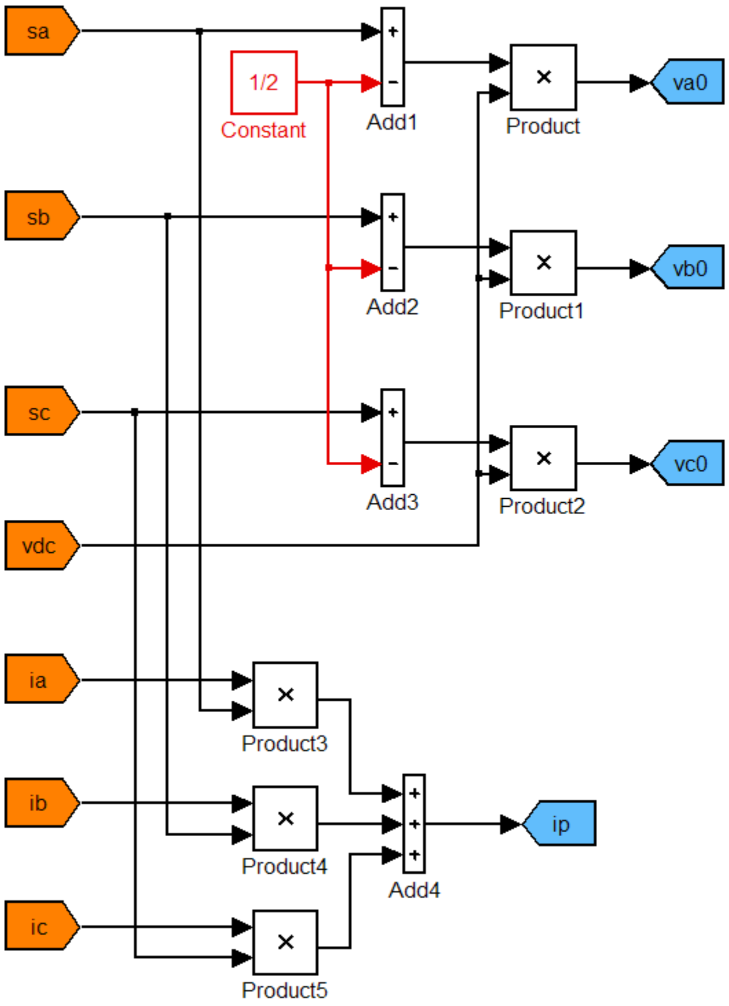


Converter

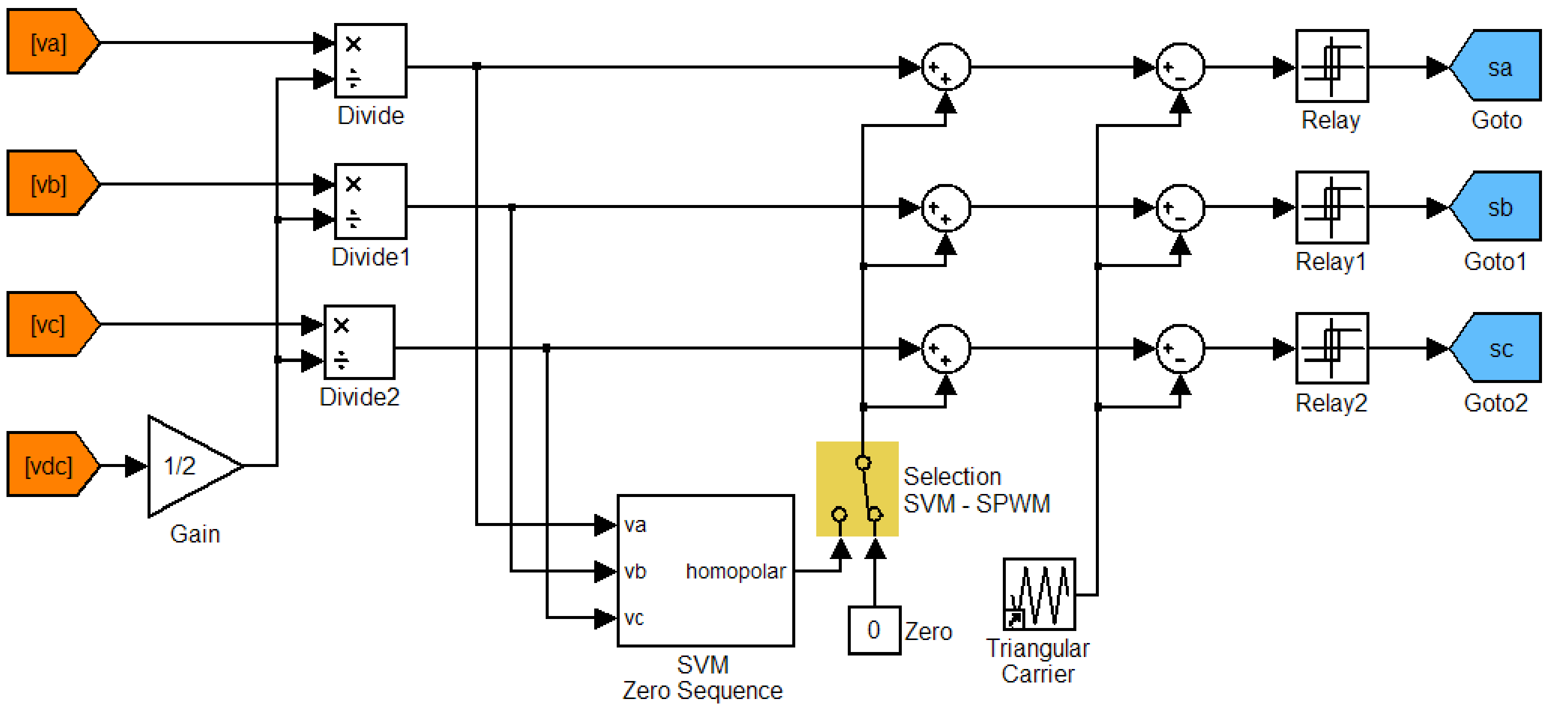
$$\begin{cases} v_{a0} = (s_a - \frac{1}{2})v_{dc} \\ v_{b0} = (s_b - \frac{1}{2})v_{dc} \\ v_{c0} = (s_c - \frac{1}{2})v_{dc} \\ i_p = s_a i_a + s_b i_b + s_c i_c \end{cases}$$



Matlab-Simulink Model

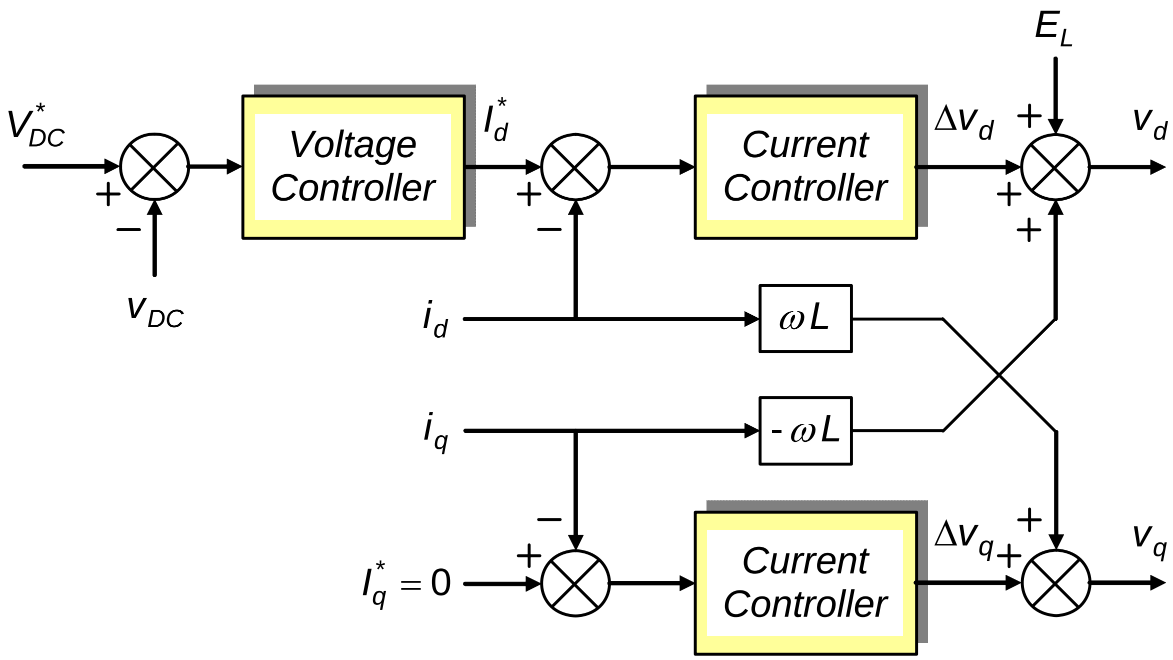


Modulation (Sinusoidal PWM)

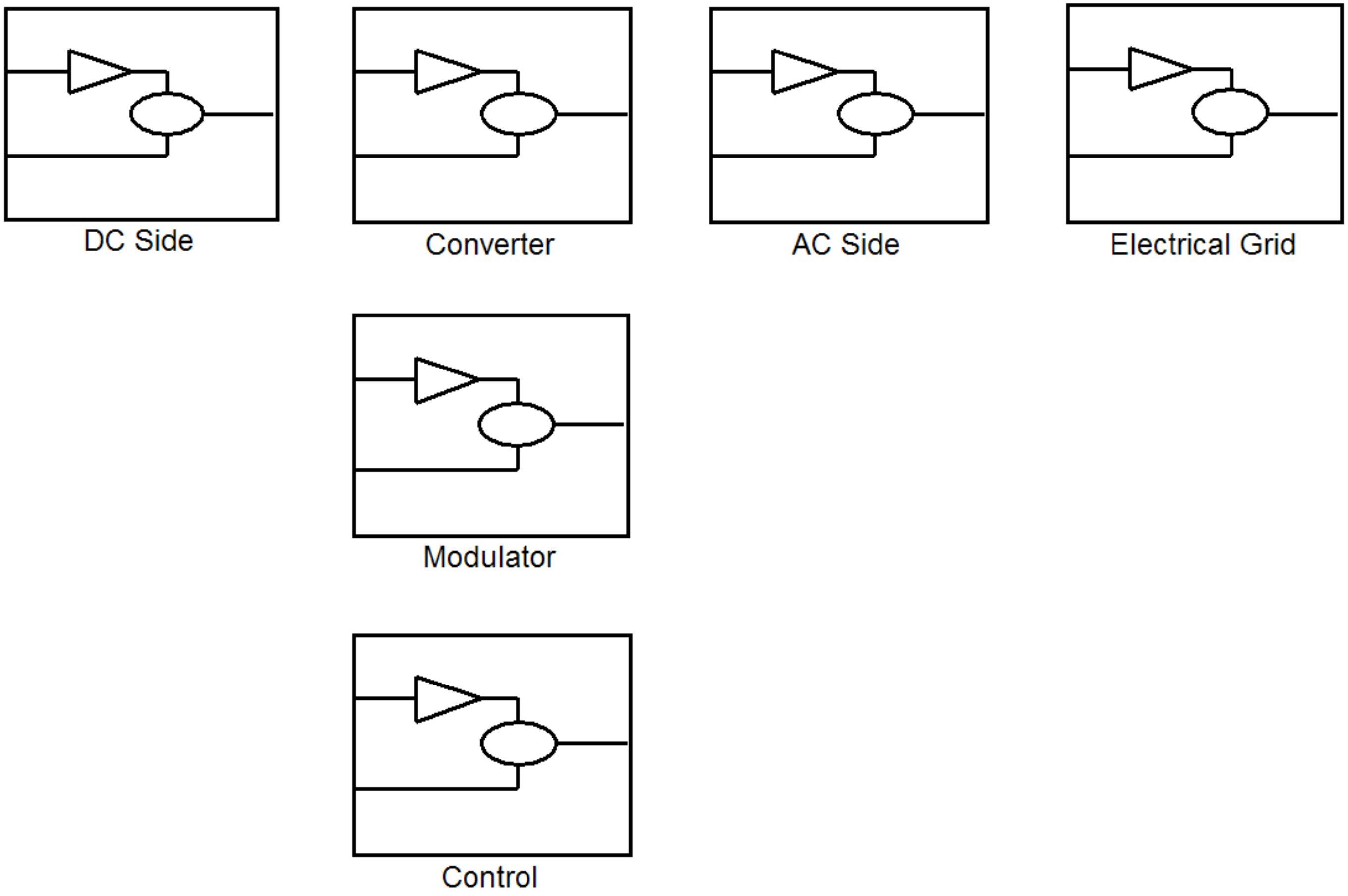


Control

Voltage Oriented Control (VOC)



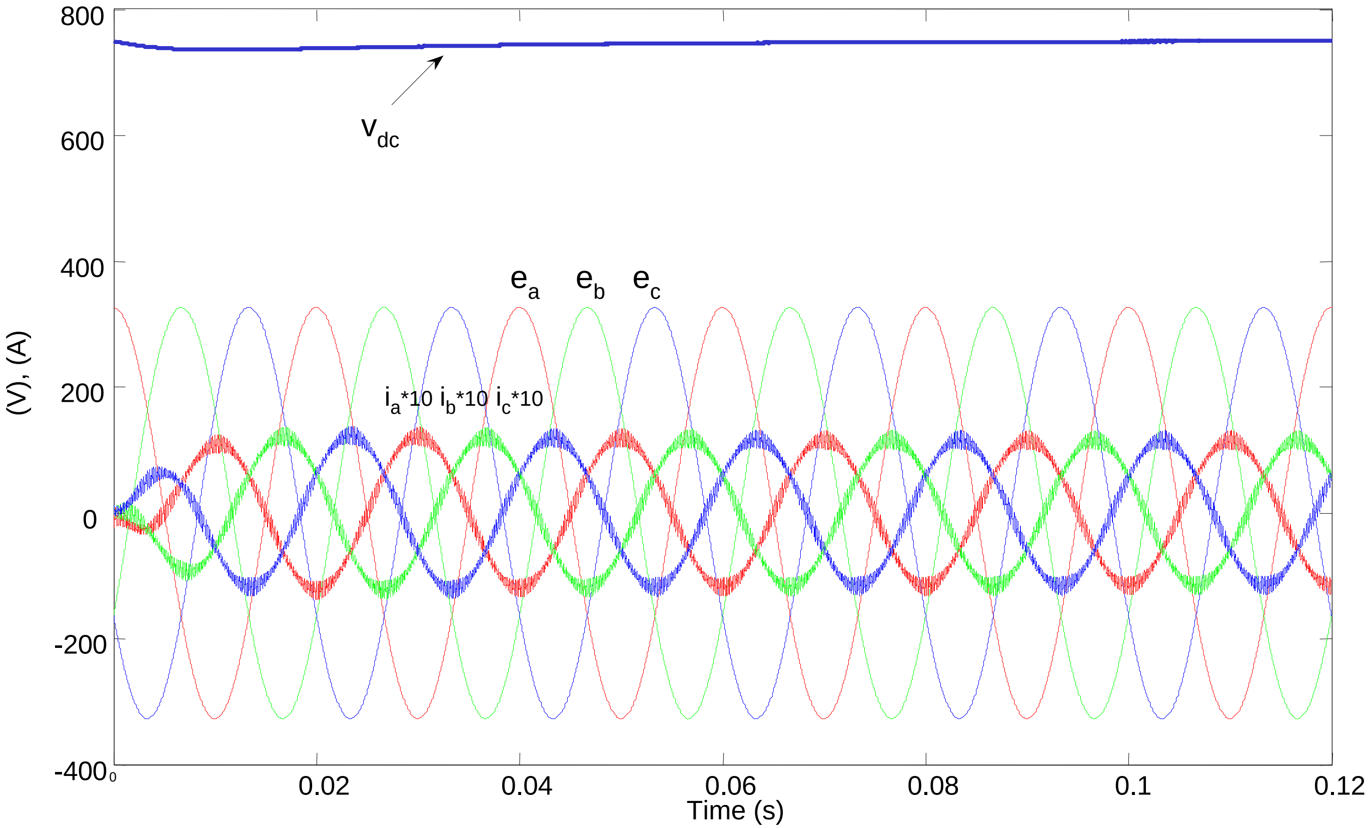
Simulation Program



Simulation Results

Main data: V_{LRMS}=400V, f=50Hz, L=6mH, R=0.1Ω, C=2200μF, V_{dc}*=750 V, f_s=5kHz.

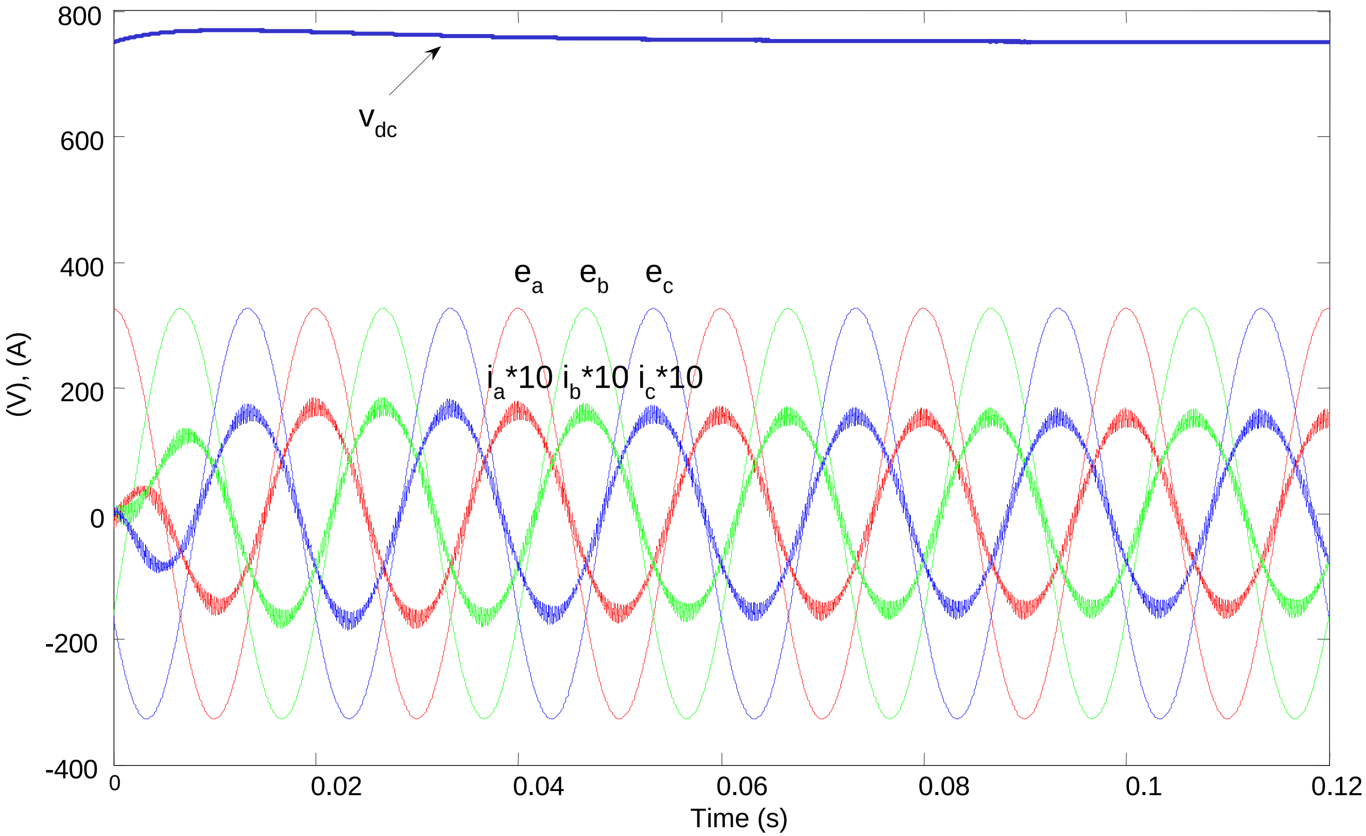
Particular data: R_p=100Ω, I_{dc}=0, I_q*=0



Simulation Results

Main data: V_{LRMS}=400V, f=50Hz, L=6mH, R=0.1Ω, C=2200μF, V_{dc}*=750 V, f_s=5kHz.

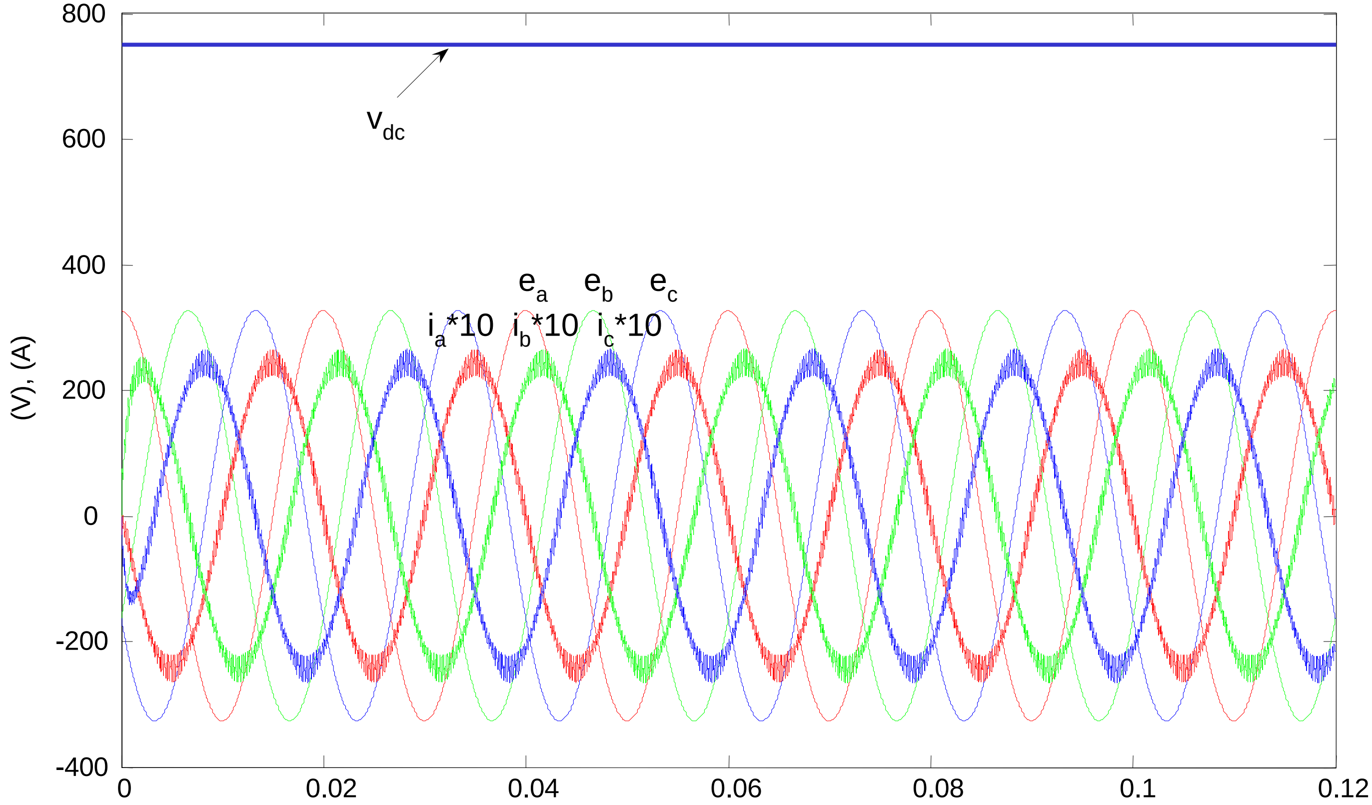
Particular data: R_p=10kΩ, I_{dc}=10A, I_q*=0



Simulation Results

Main data: V_{LRMS}=400V, f=50Hz, L=6mH, R=0.1Ω, C=2200μF, V_{dc}*=750 V, f_s=5kHz.

Particular data: R_p=10kΩ, I_{dc}=0, I_q*=20A



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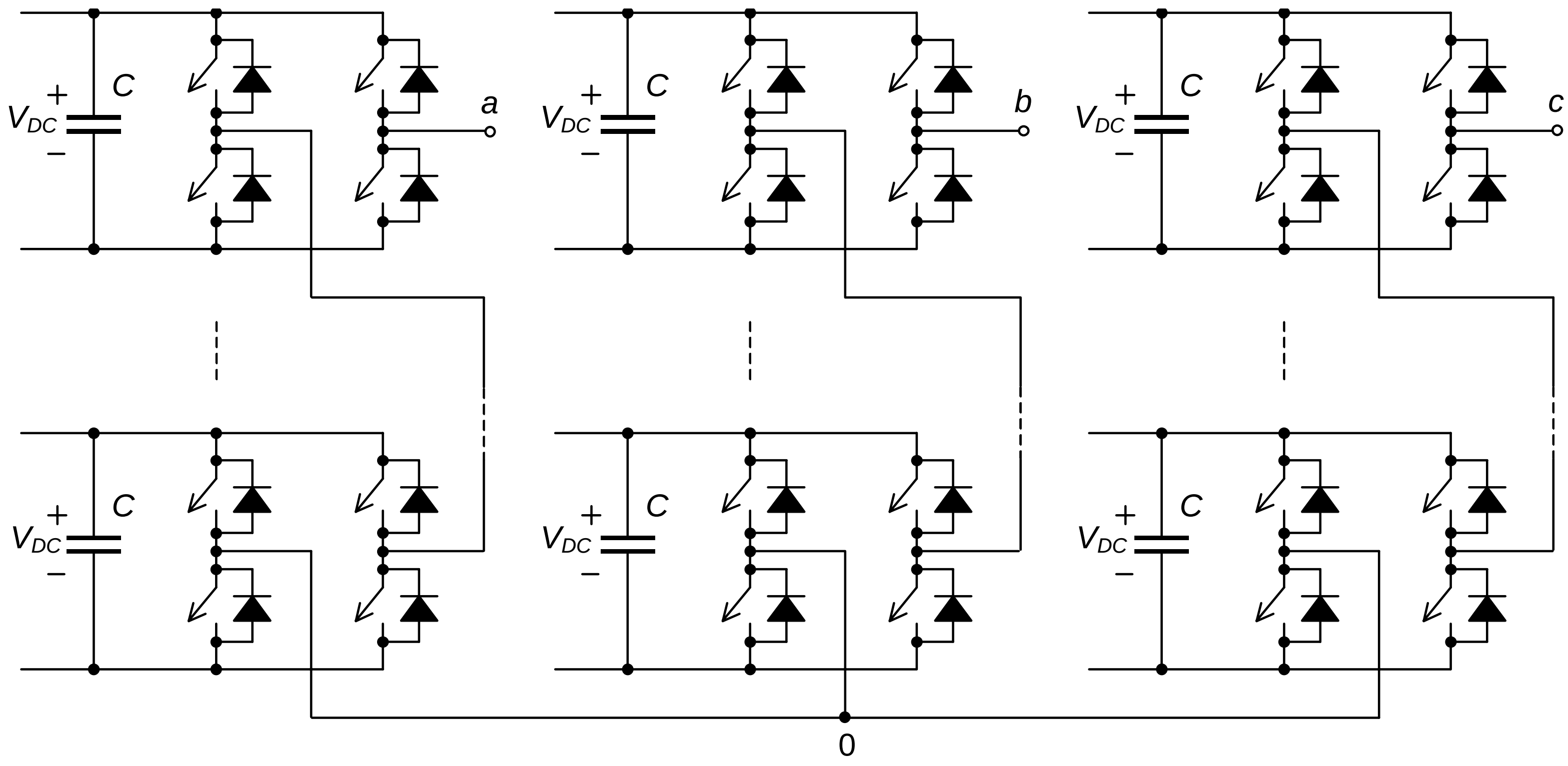
2. Multilevel Inverters

- Multilevel inverters can provide more than two voltage levels at the outputs.
- Main advantages compared with the two-level inverter:

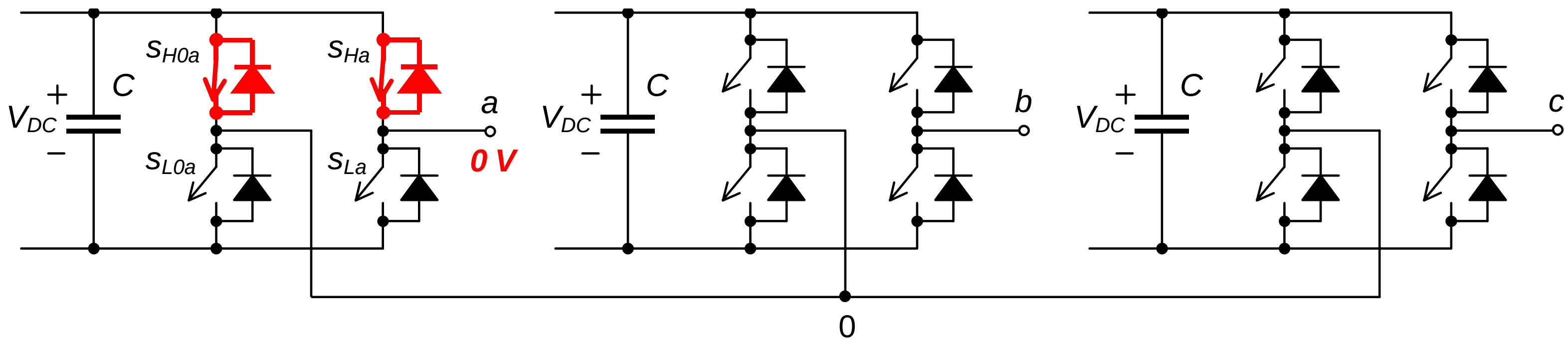
  - high quality of the output voltage spectra and
  - larger voltages that can be handled.
- Suitable for high-power applications.
- Main multilevel topologies:

  - (1) cascade H-bridge inverter,
  - (2) floating-capacitor inverter, and
  - (3) diode-clamped inverter.

(1) Cascade H-Bridge Inverters



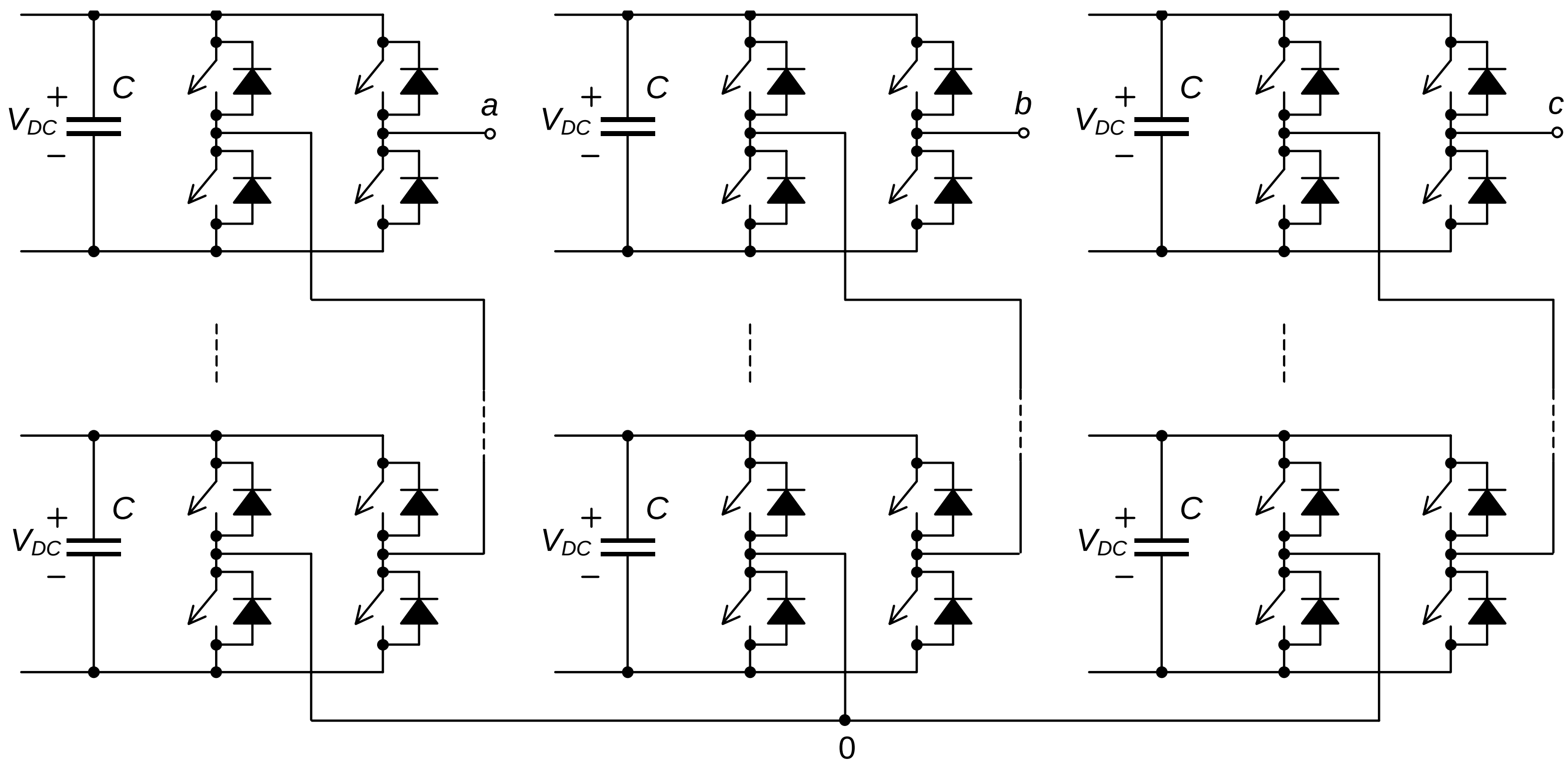
Three-Level Basic Structure



Control functions: s_{H0a} and s_{Ha}

s_{H0a}	s_{Ha}	v_{a0}
off	off	0
off	on	$+V_{DC}$
on	off	$-V_{DC}$
on	on	0

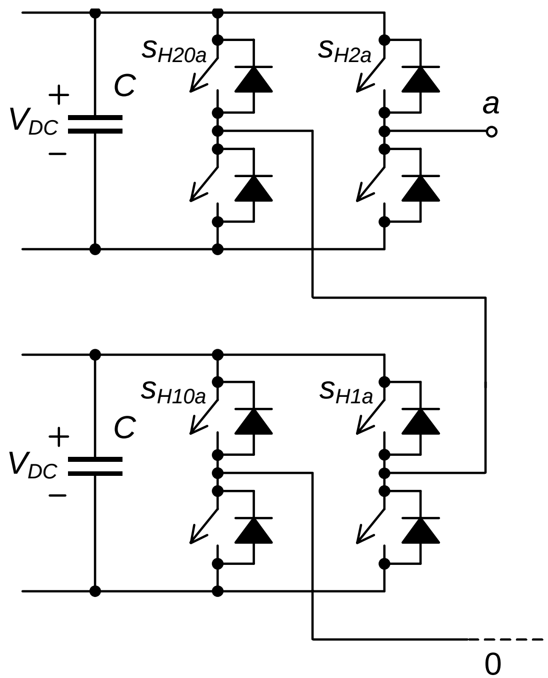
Even Number of Levels



$n = 2h+1$

n: number of output levels (per phase)
h: number of cascaded H cells

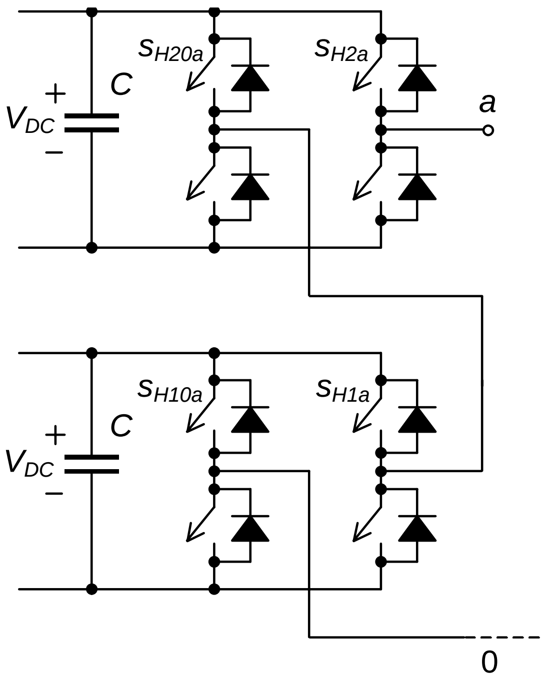
Cascaded Five-Level Inverter

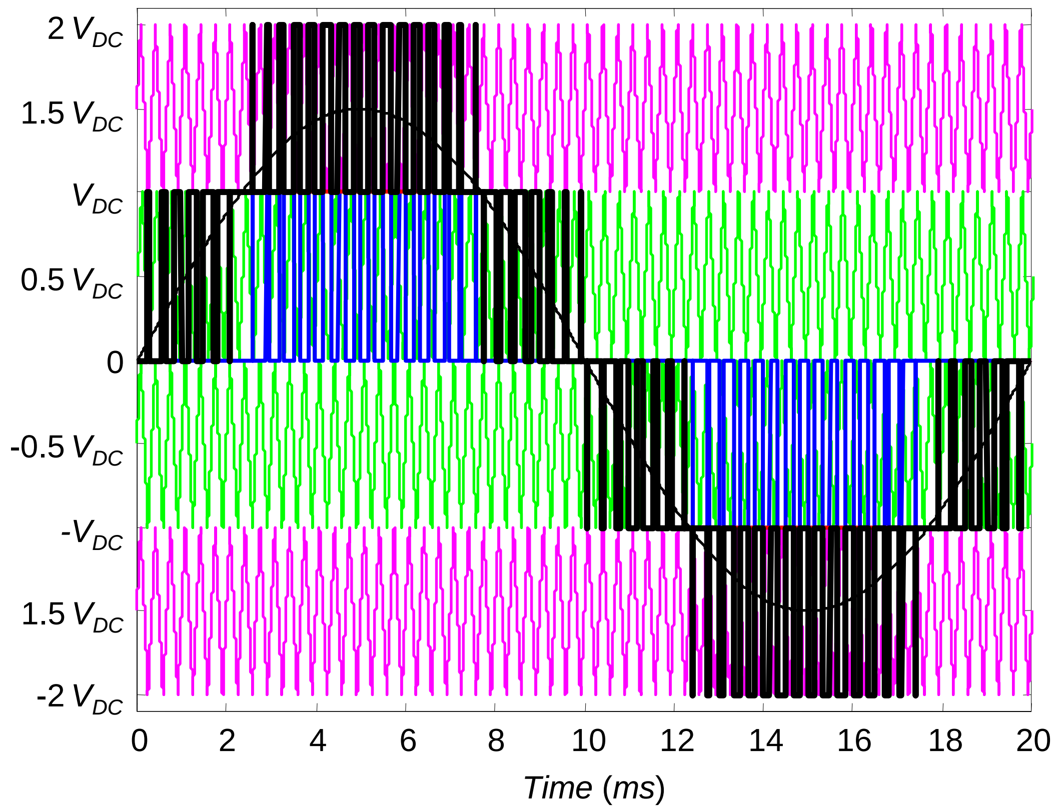


S_{H20a}	S_{H2a}	S_{H10a}	S_{H1a}	V_{a0}
off	off	off	off	0
off	off	off	on	$+V_{DC}$
off	off	on	off	$-V_{DC}$
off	off	on	on	0
off	on	off	off	$+V_{DC}$
off	on	off	on	$+2V_{DC}$
off	on	on	off	0
off	on	on	on	$+V_{DC}$
on	off	off	off	$-V_{DC}$
on	off	off	on	0
on	off	on	off	$-2V_{DC}$
on	off	on	on	$-V_{DC}$
on	on	off	off	0
on	on	off	on	$-V_{DC}$
on	on	on	off	$+V_{DC}$
on	on	on	on	0

Modulation Techniques

Example: Sinusoidal PWM (SPWM) in a Five-Level Inverter



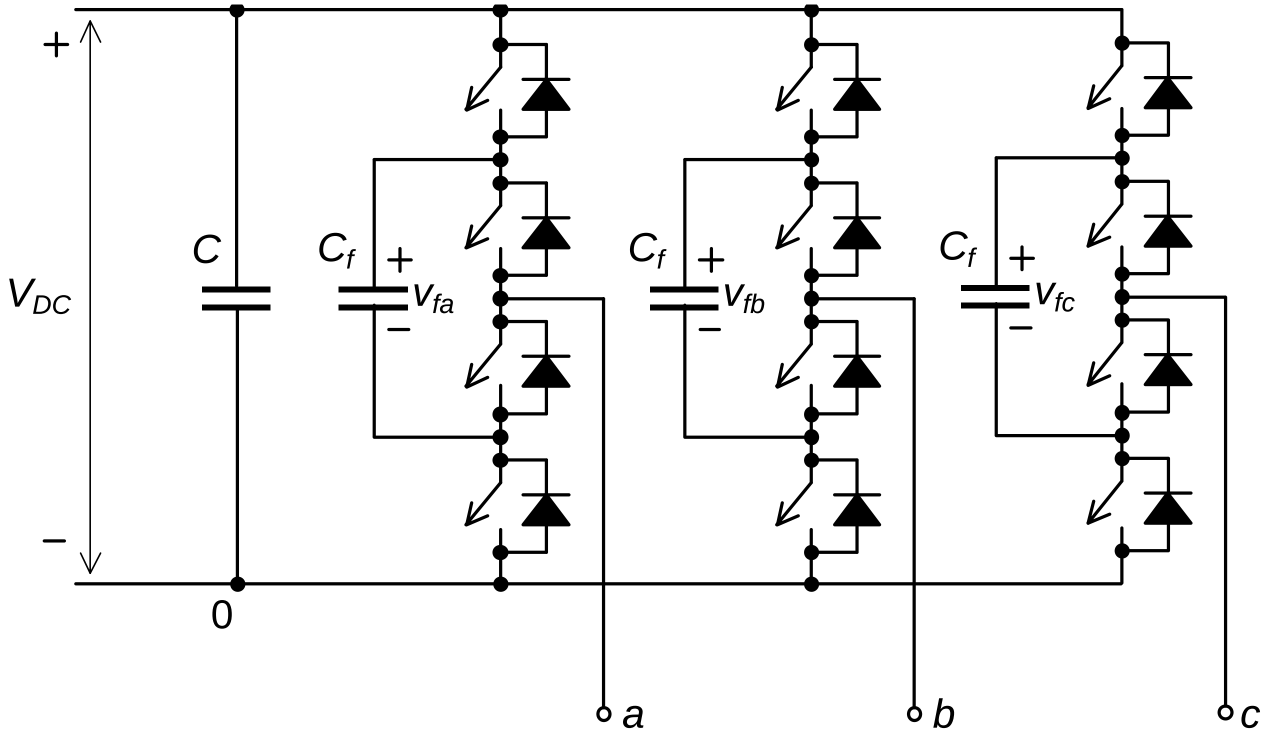


Main Features

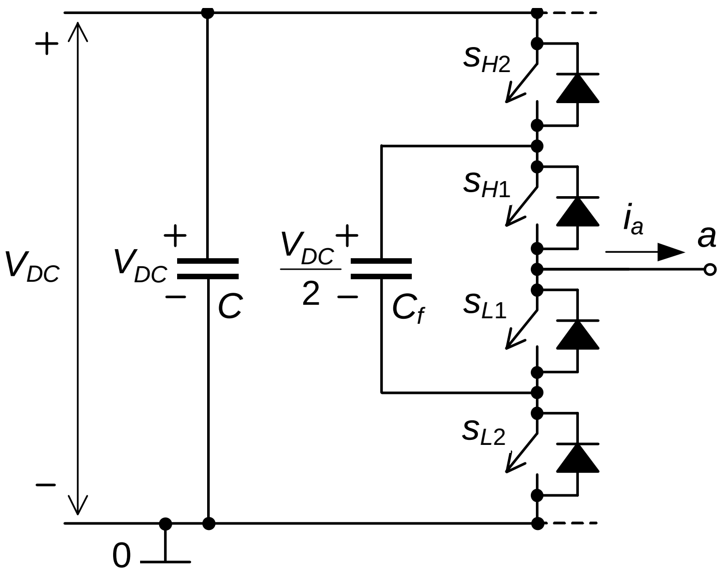
- Modular topologies. Very interesting for practical implementation.
- Main drawback: isolated DC voltage sources are required.
- Isolation is not necessary for applications such as active filtering and reactive compensation. In those cases, capacitors are used to provide DC voltages. Their voltages have to be controlled using redundant states of the converter.
- As many unities as necessary can be connected in cascade. Therefore, any AC voltage level can be achieved.

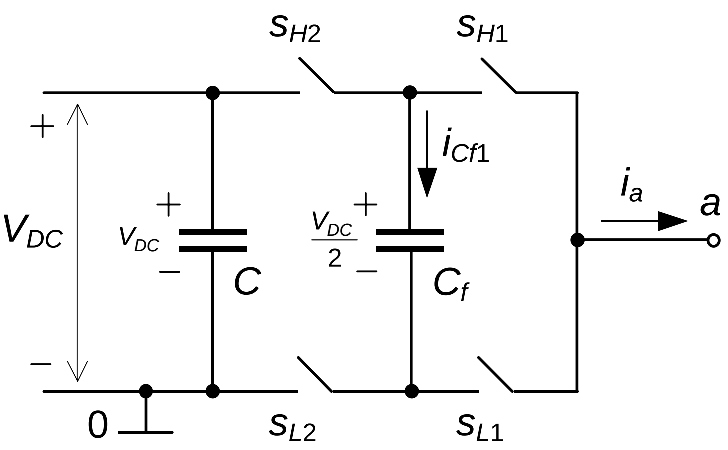
(2) Flying-Capacitor (FC) Multilevel Inverter

Three-level Topology



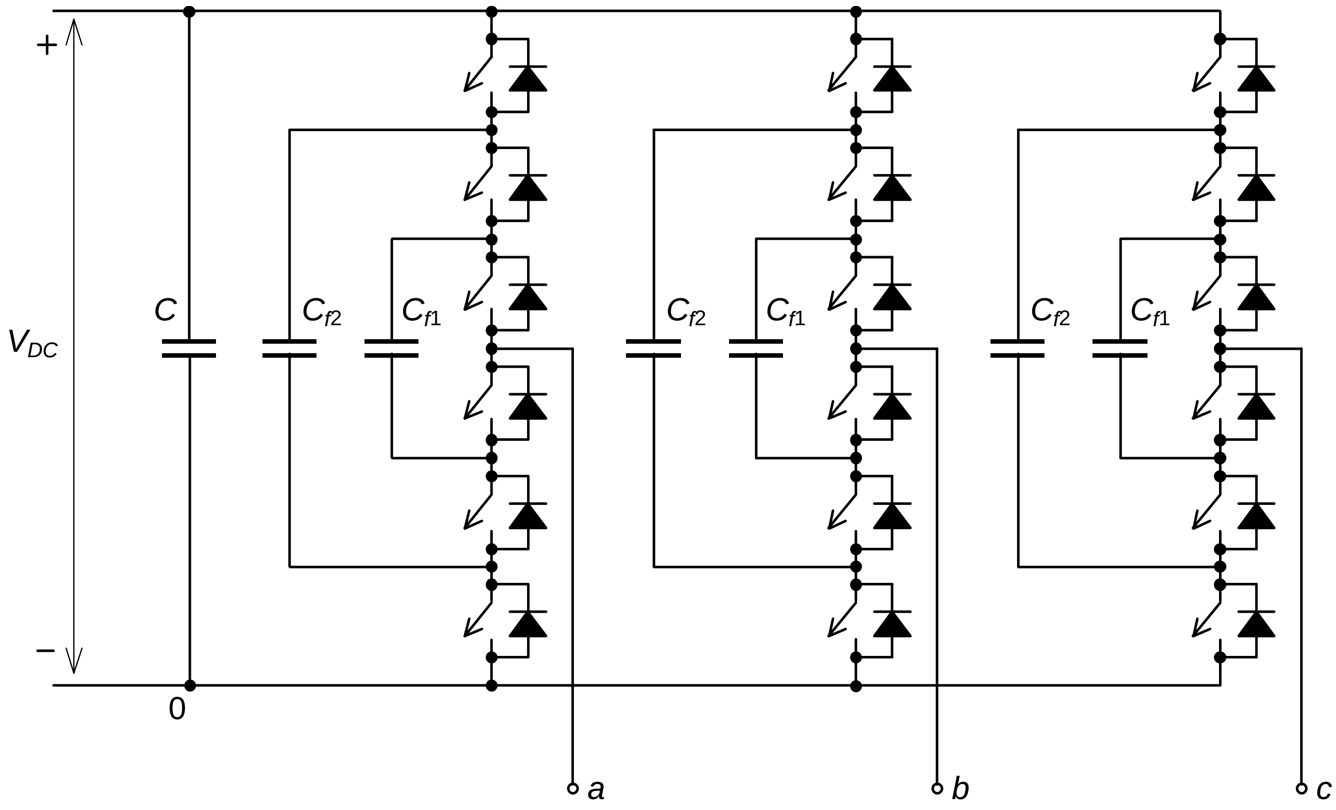
Imbricate Cells



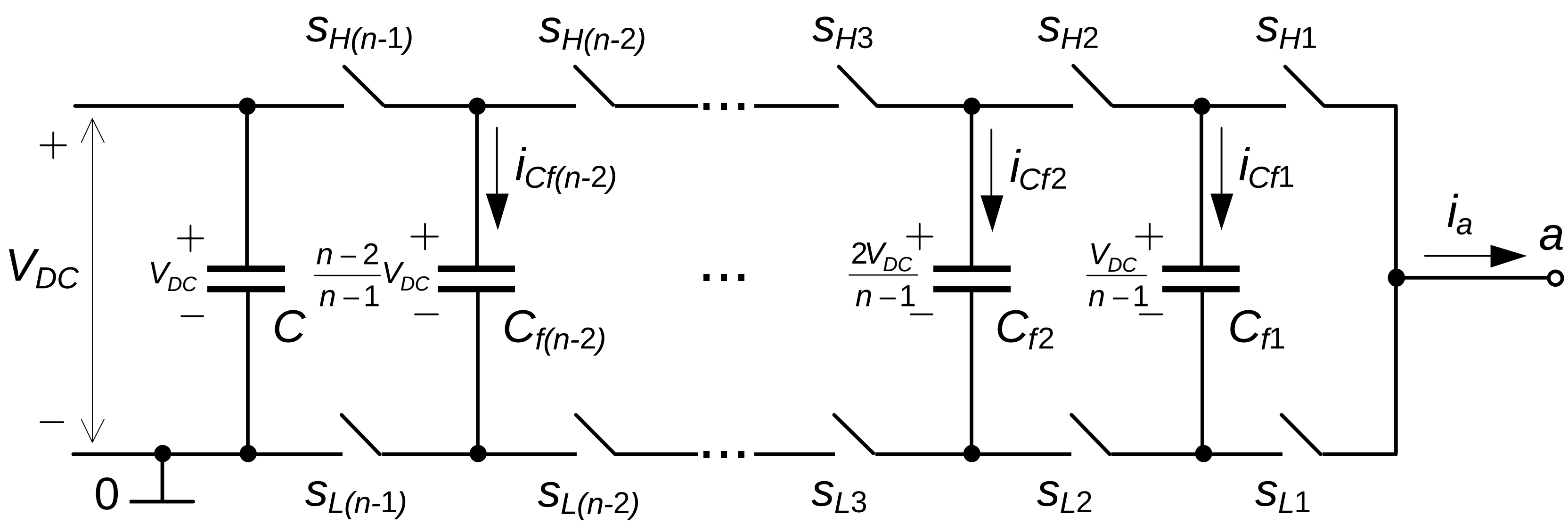


- Each leg of the converter is made up from a set of cells (imbricate cells). The output voltage is synthesized by connecting a number of cells (capacitors) in series.
- S_{Hi} and S_{Li}, with i = {1, 2}, must be in opposite states to avoid short-circuits.

FC Four-Level Topology



Imbricate Cells in an *n*-level FC Inverter



- Voltages on the floating capacitors are different.

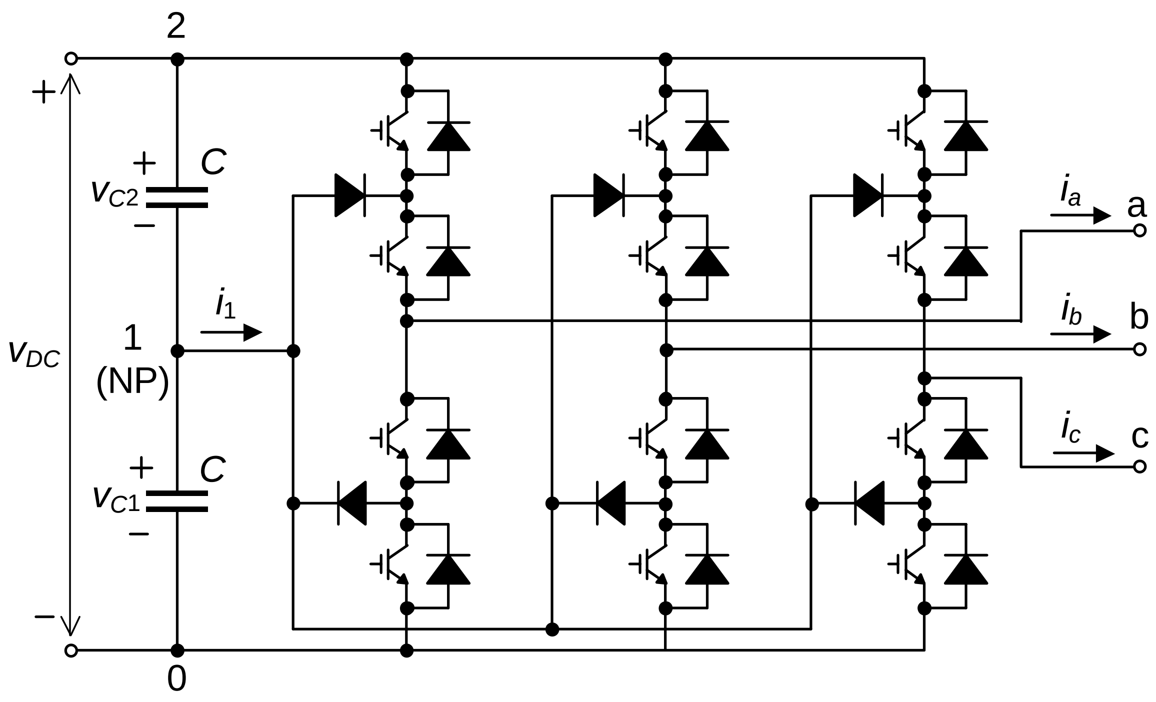
Main Features

- FC multilevel topologies require a large number of capacitors, specially in high-order structures (n>3).
- Precharge of the flying capacitors is required.
- Voltages on the flying capacitors can be controlled. Each leg regulates the voltages on their capacitors independently of the others.

(3) Diode-Clamped Inverters

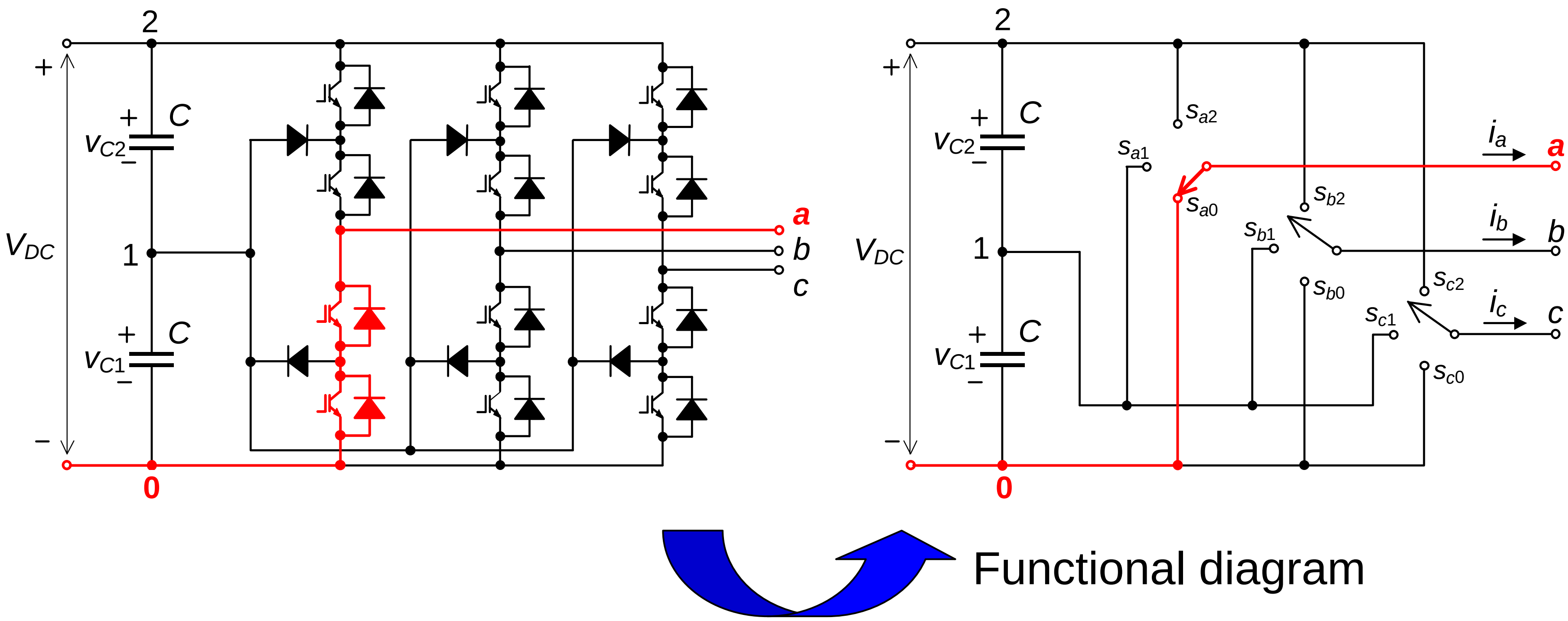
Three-level diode-clamped inverter =

Neutral-Point-Clamped (NPC) Inverter



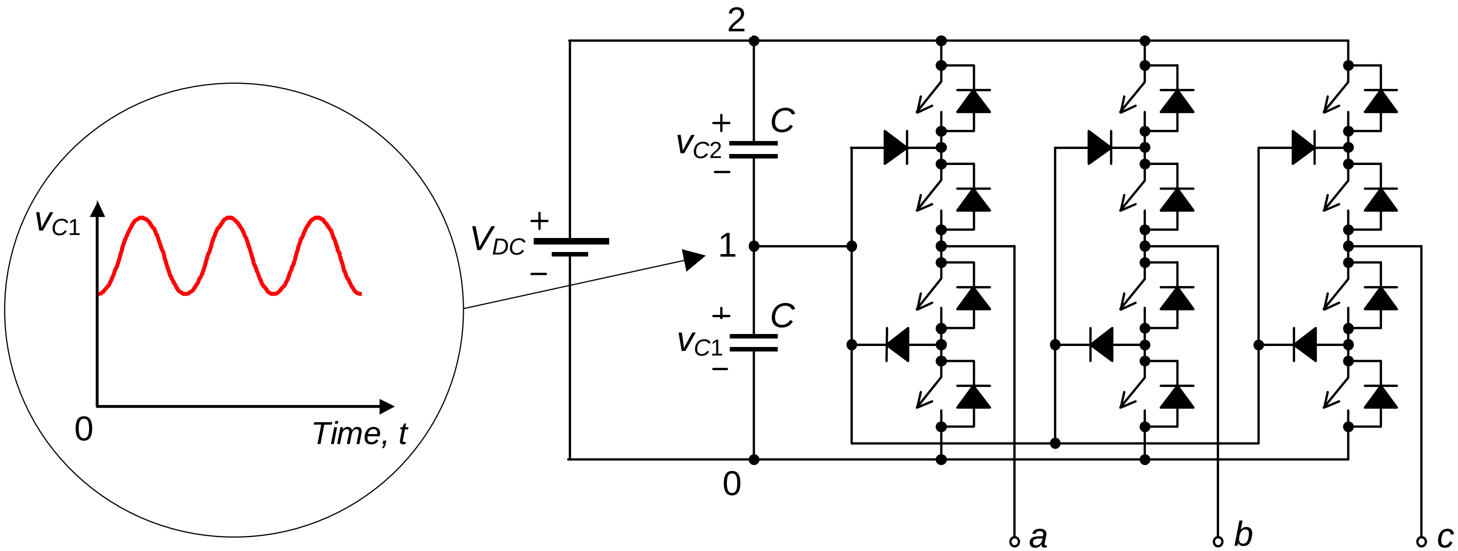
NPC Inverter

Operation principles



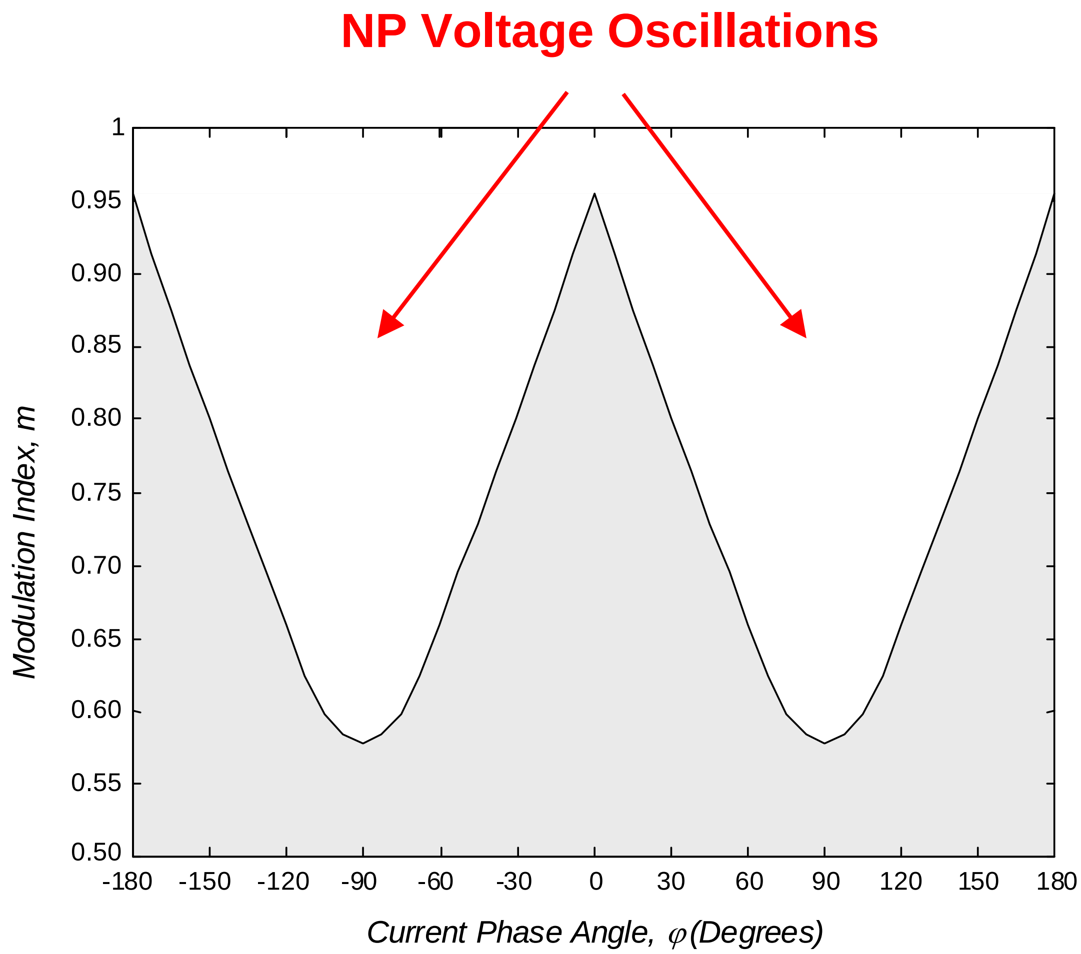
Two consecutive switches must be in on-state

Neutral-Point Voltage Oscillations



A low-frequency oscillation may appear in the neutral-point (NP) voltage.

Oscillation Area

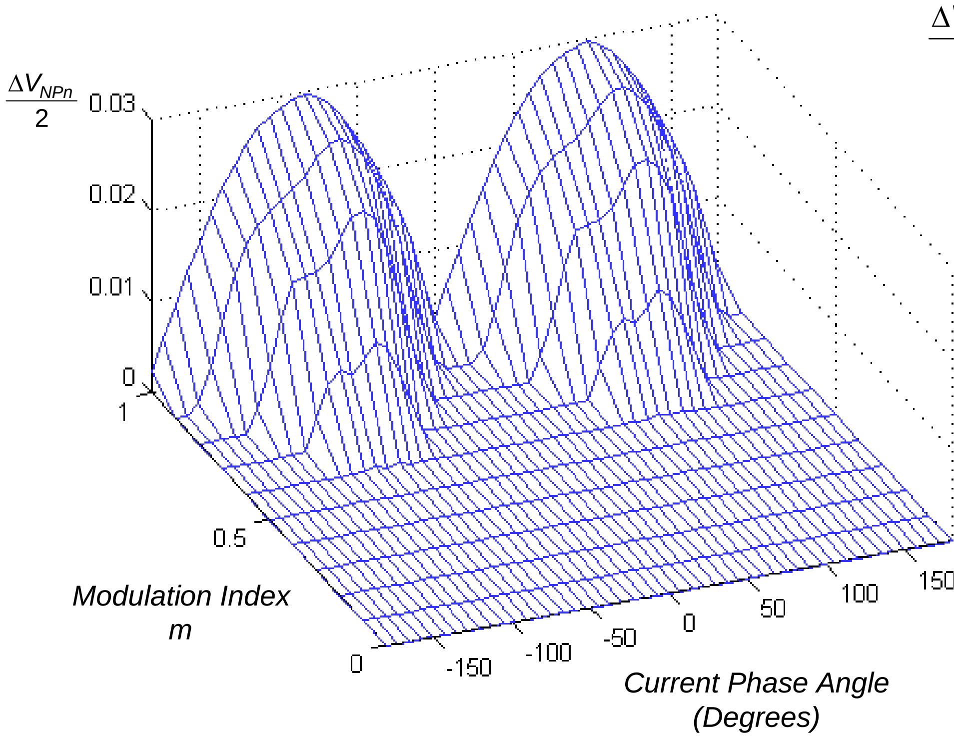


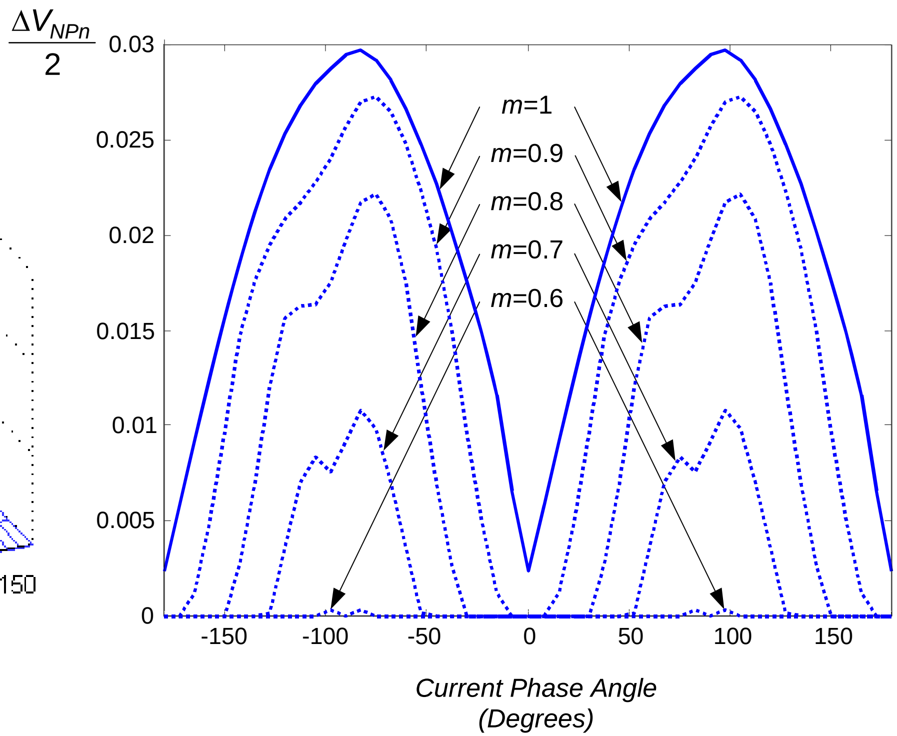
Voltage Oscillation Amplitude

Normalized amplitude of the NP voltage ripple ($\Delta V_{NPn}/2$):

$$\frac{\Delta V_{NPn}}{2} = \frac{\Delta V_{NP}/2}{I_{RMS}/fC}$$

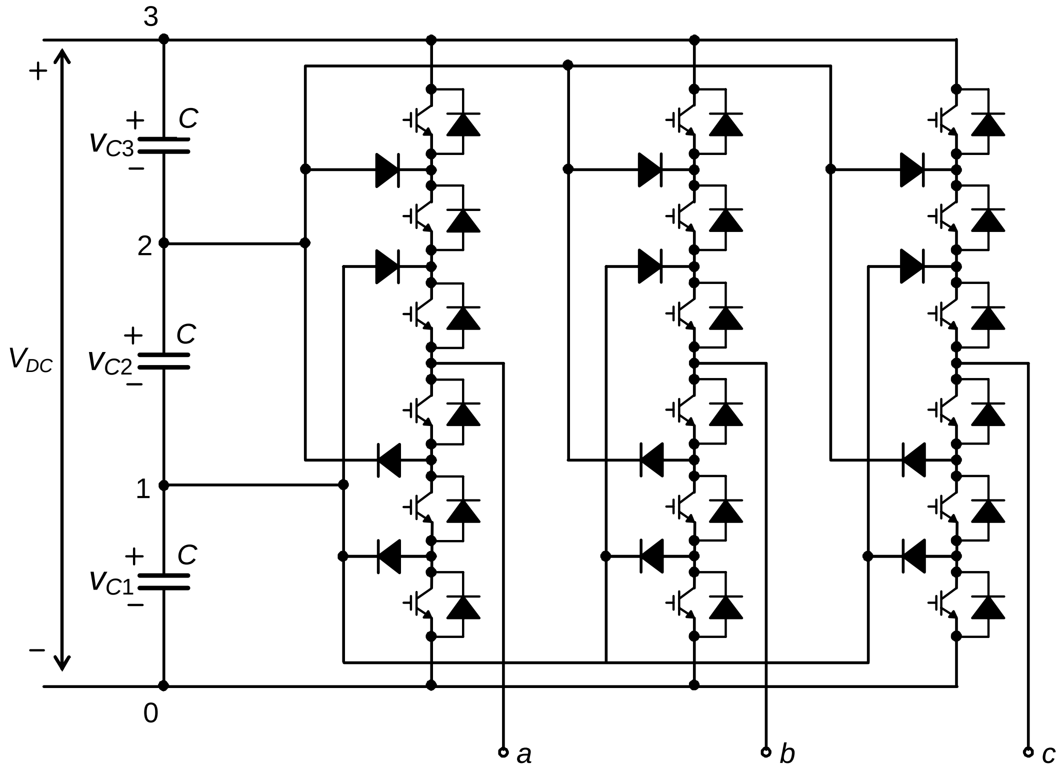
- $\Delta V_{NP}/2$: amplitude of the NP voltage ripple
- I_{RMS}: RMS output current
- f: line frequency
- C: value of the DC-link capacitors





Four-Level Diode-Clamped Inverter

Four-level topology

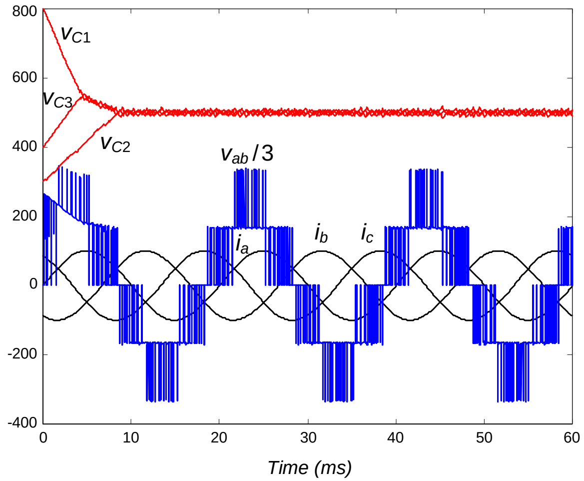


Four-Level Multilevel Inverter

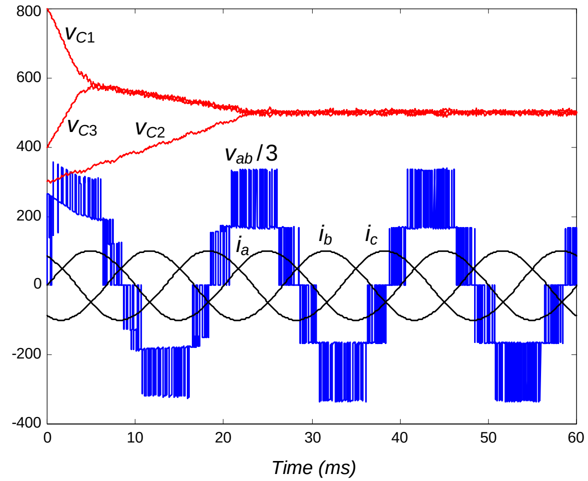
Voltage balance problems

Example operating under unity power factor

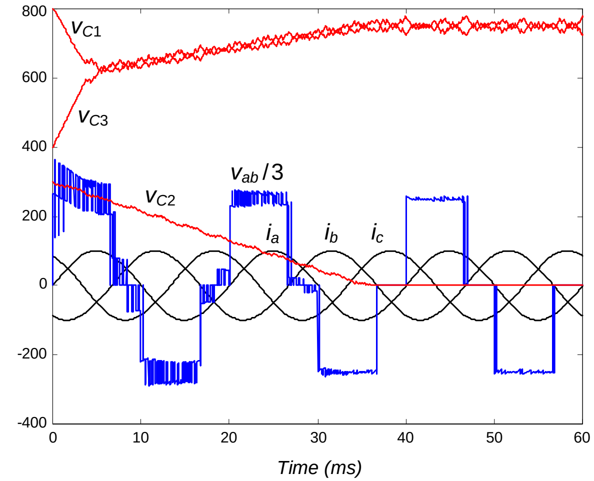
m=0.4



m=0.5

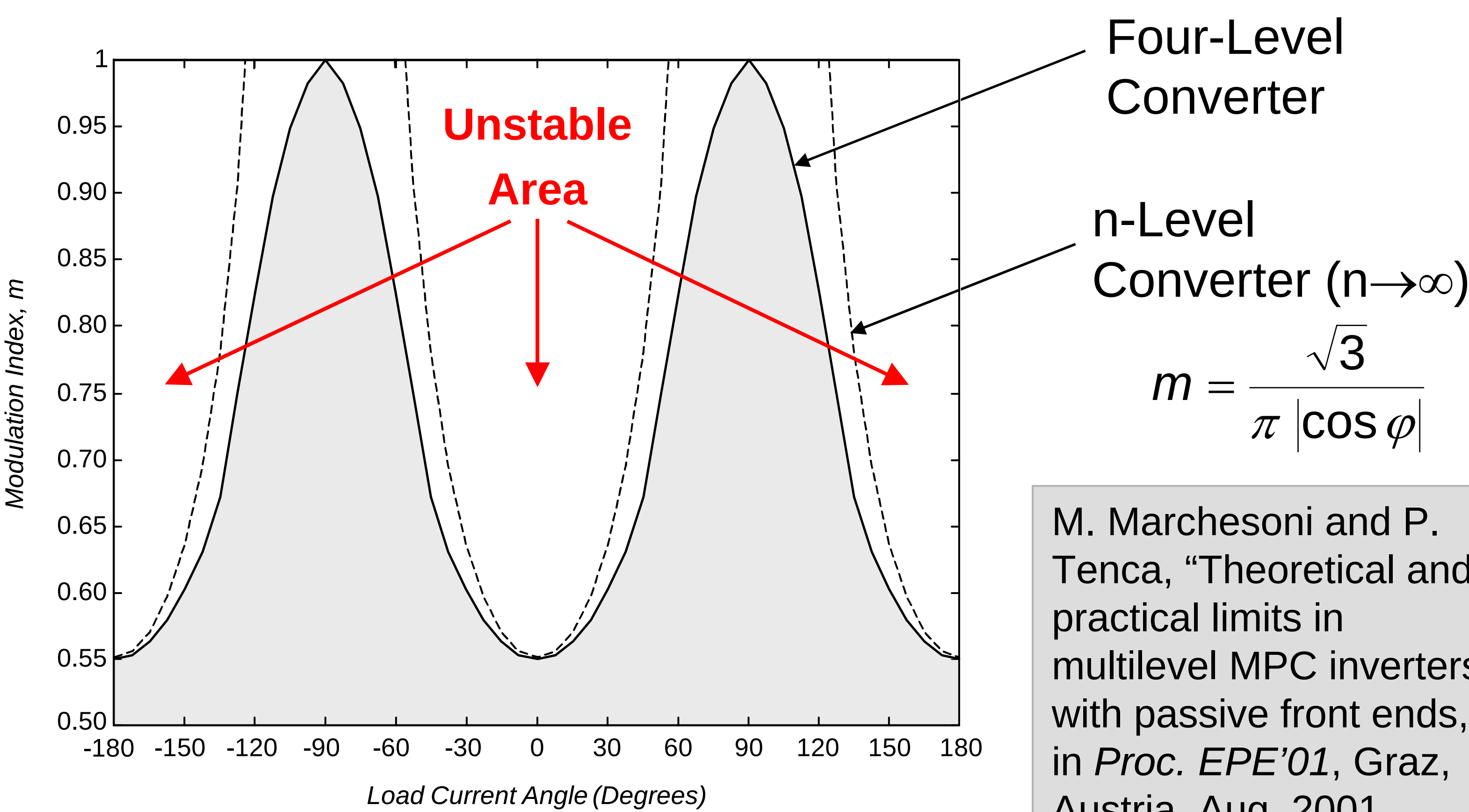


m=0.6



J. Pou, R. Pindado, and D. Boroyevich, "Voltage-Balance Limits in Four-Level Diode-Clamped Converters With Passive Front Ends," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 190-196, Feb. 2005.

Limits of Voltage Balance



$$m = \frac{\sqrt{3}}{\pi \left|\cos\varphi\right|}$$

M. Marchesoni and P. Tenca, "Theoretical and practical limits in multilevel MPC inverters with passive front ends," in *Proc. EPE'01*, Graz, Austria, Aug. 2001.

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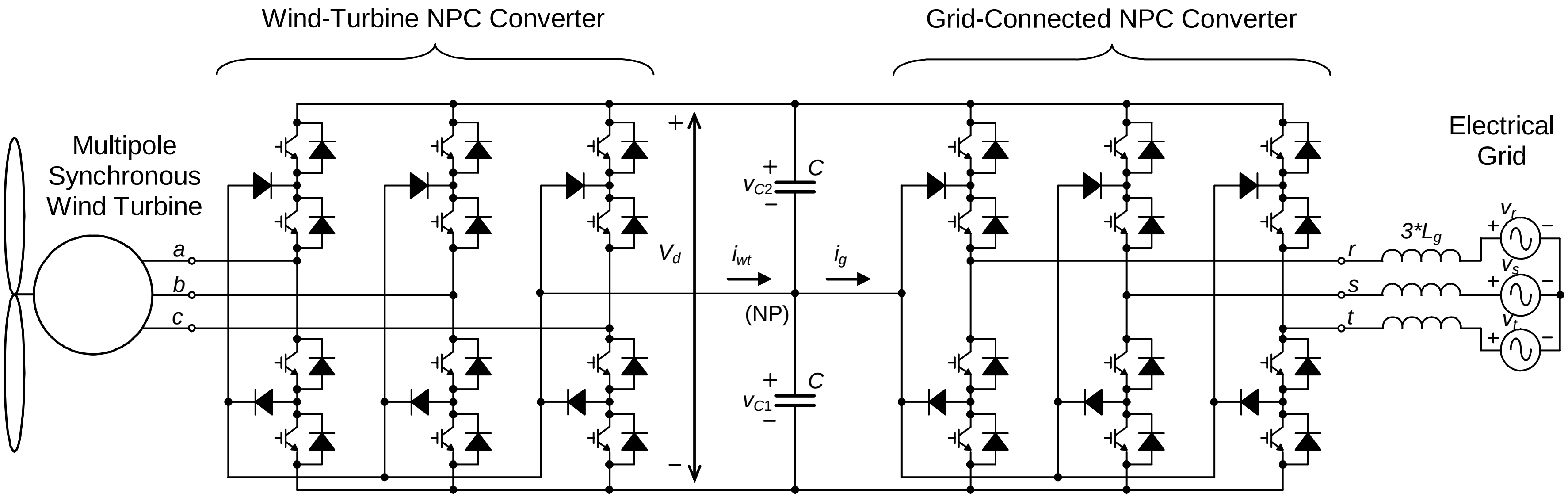
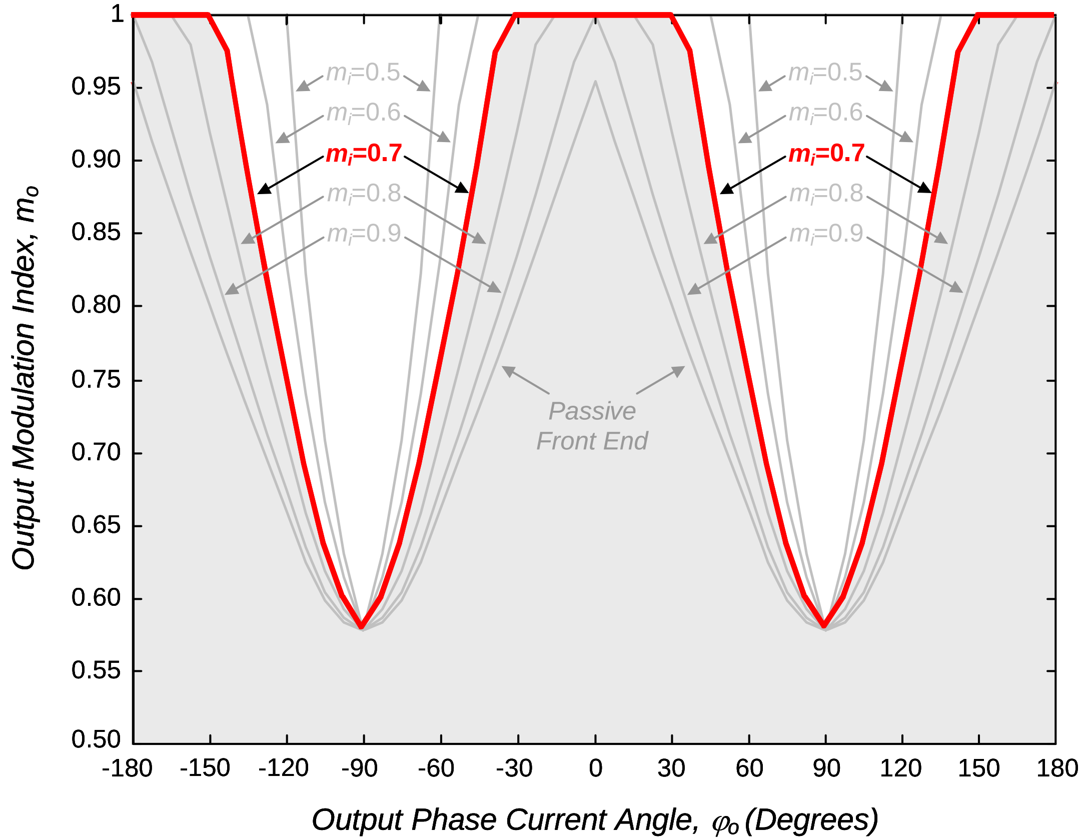
AC-DC-AC NPC-Based System



- Back-to-back-connected NPC converters. Example of application to MPSG wind turbines.

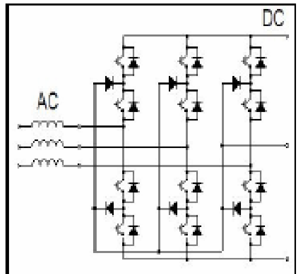
Voltage-balance Improvements



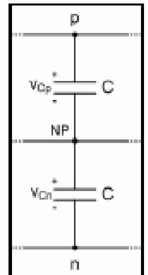
Conditions: constant output current (I_{RMSo}=ct.), unity input power factor (φ_i=0º, 180º), and 100% efficiency (η=1).

Matlab-Simulink Simulation Platform

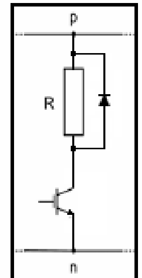
ELECTRICAL GRID



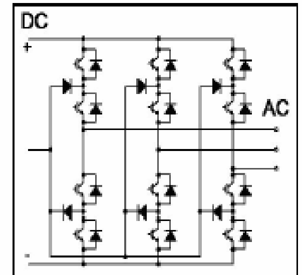
GRID-CONNECTED NPC CONVERTER



DC-LINK CAPACITORS

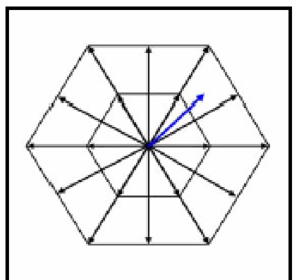


CHOPPER

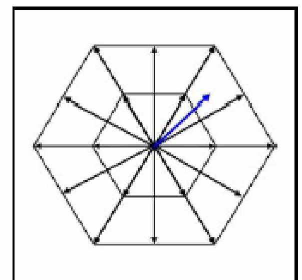


WIND-TURBINE NPC CONVERTER

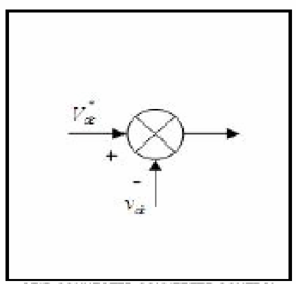
WIND GENERATOR



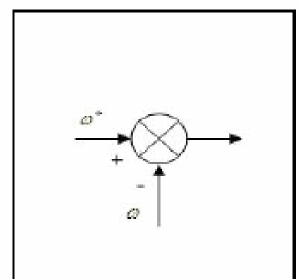
DSPWM for the
Grid-Connected NPC Converter



DSPWM for the
Wind-Turbine NPC Converter



GRID-CONNECTED CONVERTER CONTROL

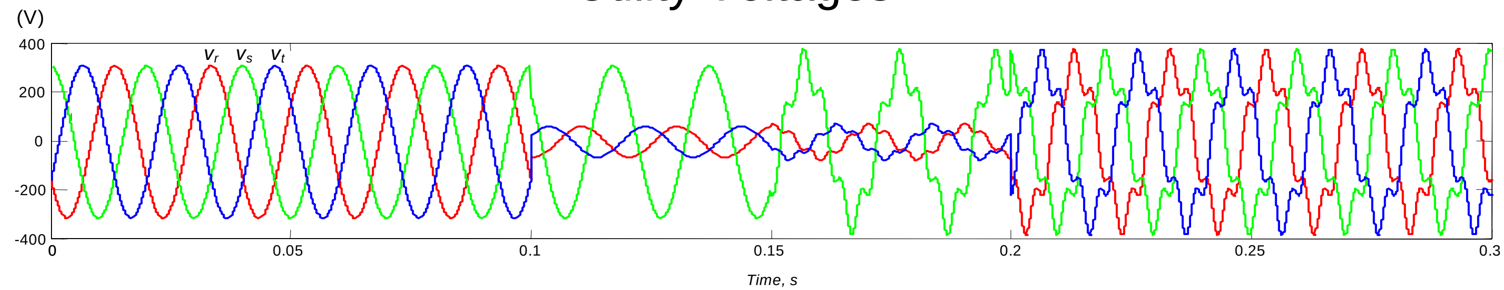


WIND TURBINE CONTROL

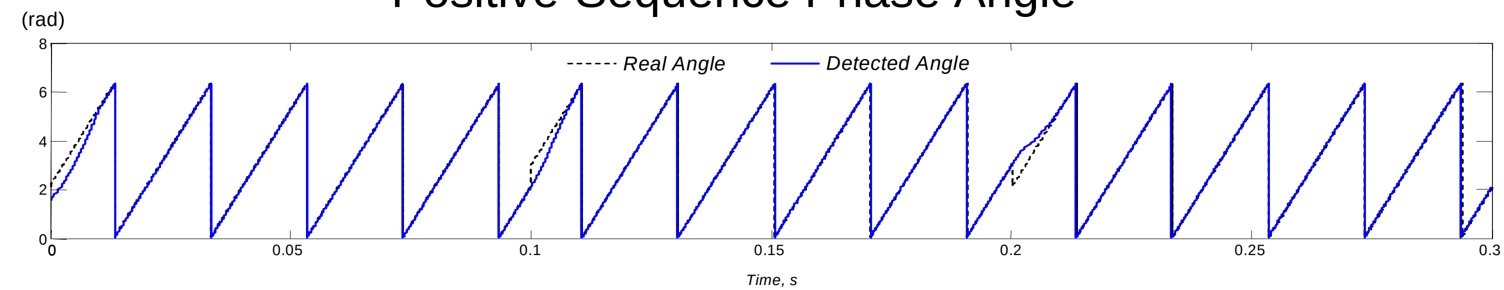
Simulation Results

Two-phase voltage dip process with a fifth harmonic

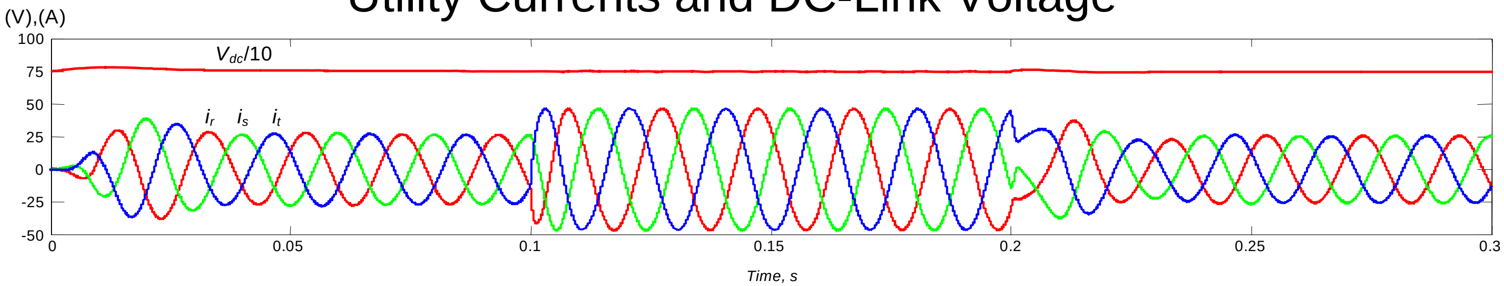
Utility Voltages



Positive-Sequence Phase Angle



Utility Currents and DC-Link Voltage



Remarks

- Multilevel topologies can be applied to high-power wind-turbine systems. They are expected to be extensively used when the wind turbines rated power reaches about 10 MW.
- Among the multilevel topologies, the three-level NPC is the most produced used nowadays. An important drawback of this topology is the voltage oscillations that may appear in the NP under some operating conditions.
- The back-to-back connection of NPCs forms an AC/DC/AC system. In such a configuration the NP voltage oscillations become significantly attenuated.